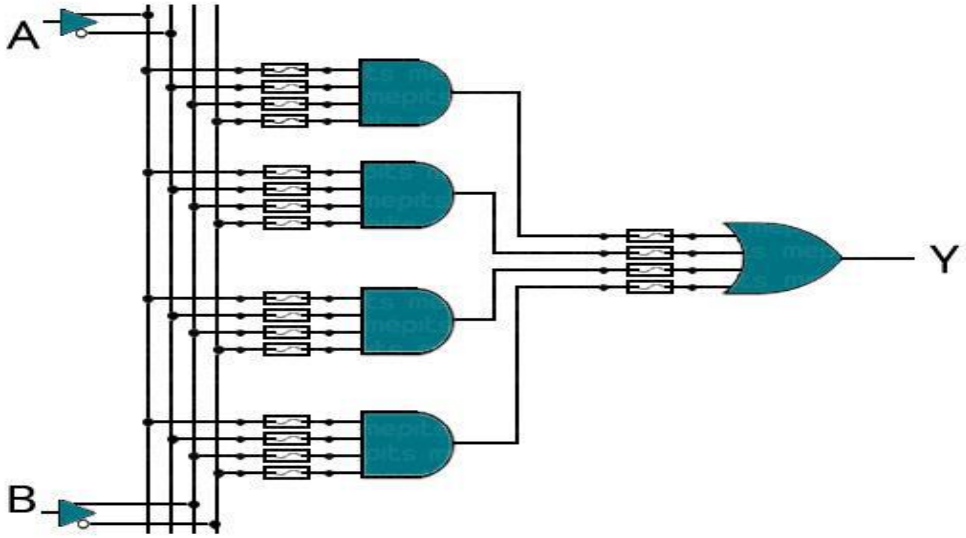
Electronic Systems Simulators

BY –KERIM .D.

SPLD SIMPLE Programmable Logic Devices

SPLD: Simple Programmable Logic Devices: A programmable, digital logic IC containing several PAL or PLA structures with internal interconnections and memory registers.



example:

$F0 = A + B' C'$

$F1 = A C' + A B$

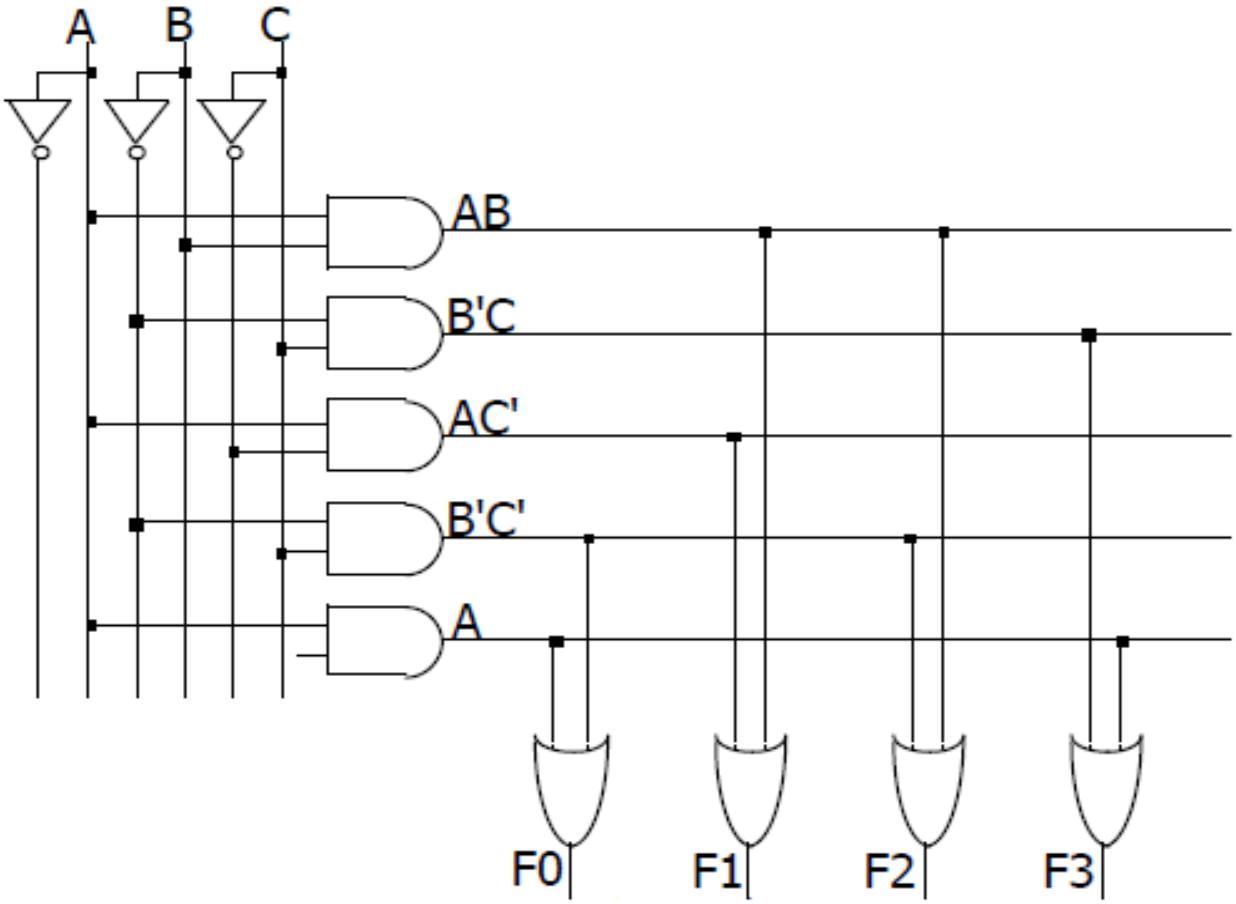
$F2 = B' C' + A B$

$F3 = B' C + A$

personality matrix

product term	inputs A	B	C	outputs F0	F1	F2	F3
AB	1	1	–	0	1	1	0
B'C	–	0	1	0	0	0	1
AC'	1	–	0	0	1	0	0
B'C'	–	0	0	1	0	1	0
A	1	–	–	1	0	0	1

reuse of terms

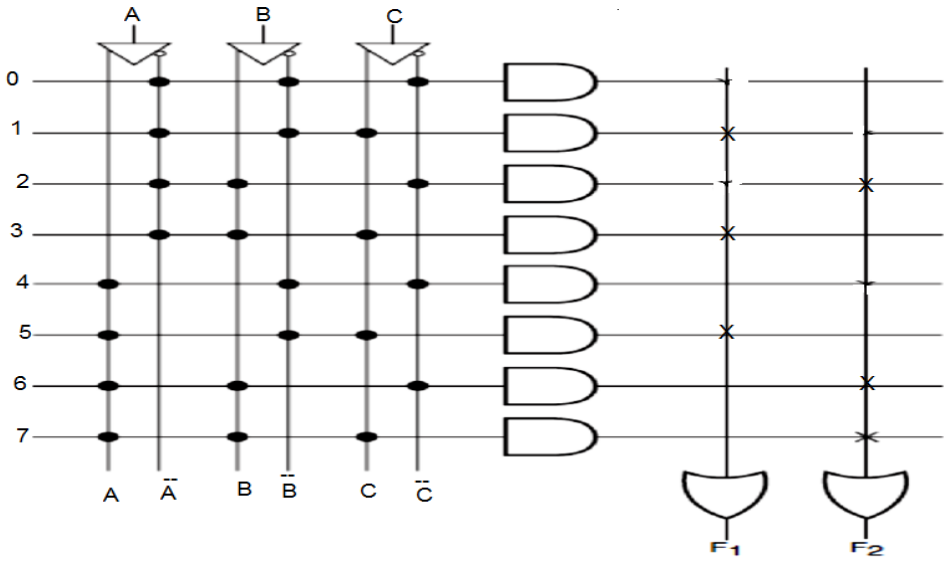


EXAMPLE :Implementation the Boolean function using 8x2 PROM

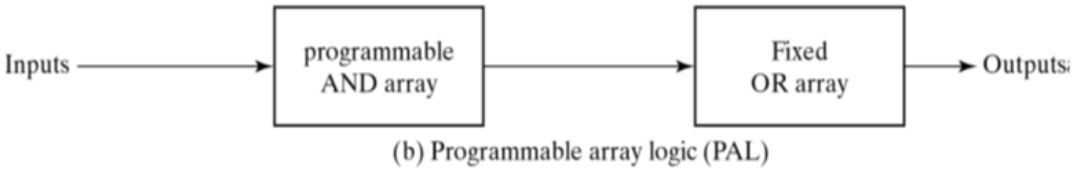
F1=∑ 1,3,5

F2=∑ 2,6,7

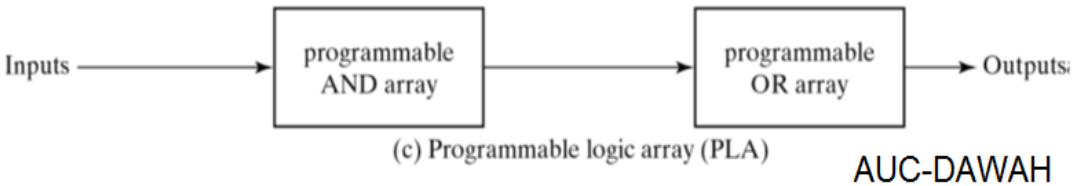
SOLUTION:



(a) Programmable read-only memory (PROM)



(b) Programmable array logic (PAL)



(c) Programmable logic array (PLA)

AUC-DAWAH

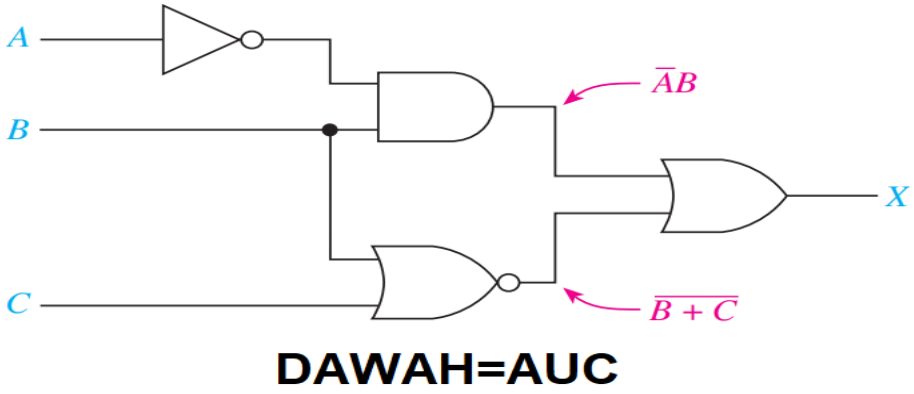
Basic Configuration of Three PLDs

PAL: Programmable Array Logic: Its basic structure contains multiple inputs to several AND gates, the outputs of which are connected to a series of fixed ORs.

PLA: Programmable Logic Array: Its basic structure contains multiple inputs to several AND gates, the outputs of which are connected to a series of programmable ORs.

PLD: Programmable Logic Device: An IC containing thousands of undefined logic functions.

To illustrate the power of a **PLD**, let's consider the logic circuit required to implement **X=A'B+**$\overline{B + C}$Figure 1 shows the circuitry required to implement the logic using 7400-series ICs. As shown, we would need four different ICs to solve this equation. Wires are shown connecting one gate of each IC to one gate of the next IC until the logic requirements are met. To solve this same logic using a PLD, we would draw the schematic or use VHDL to define the logic, then program that into a PLD. One possible PLD that could be used to implement this logic is the Altera EPM7128S (see Figure 2). (in this case) to input A, B, and C at pins 29, 30, and 31 and output to X at pin 73. The PLD software selected which pins to use, and as you can see, only a small portion of the PLD is actually used for this circuit. This particular PLD is an 84-pin IC in a plastic leaded chip carrier (PLCC) package having 21 pins on a side. The notch signifies the upper left corner of the IC. Pin 1 is located in the middle of the upper row adjacent to a small indented circle;



logic diagram

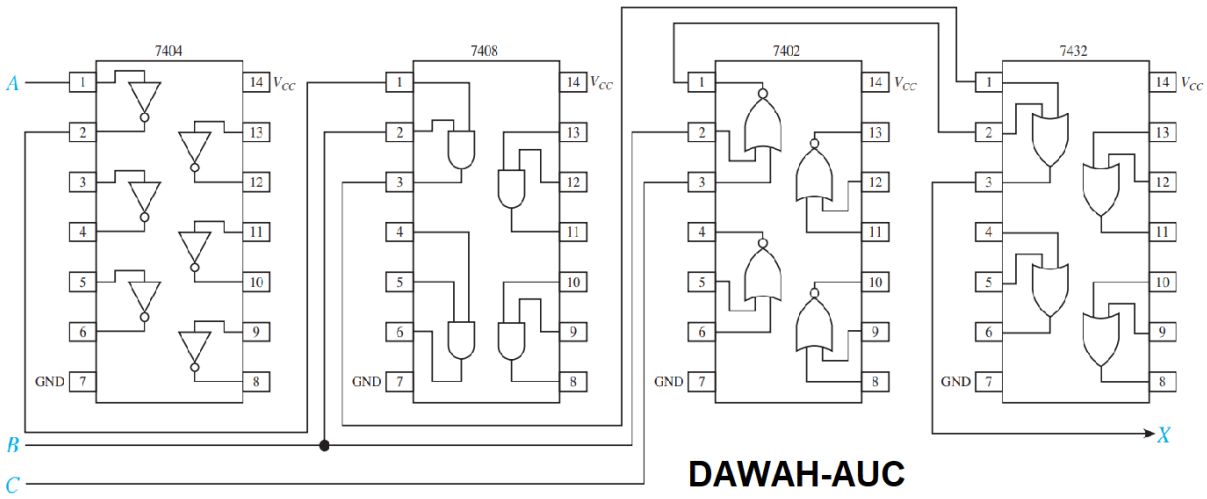


Figure 1 Implementing the equation X=A'B+$\overline{B+C}$ using 7400-series logic ICs: connections to IC chips.

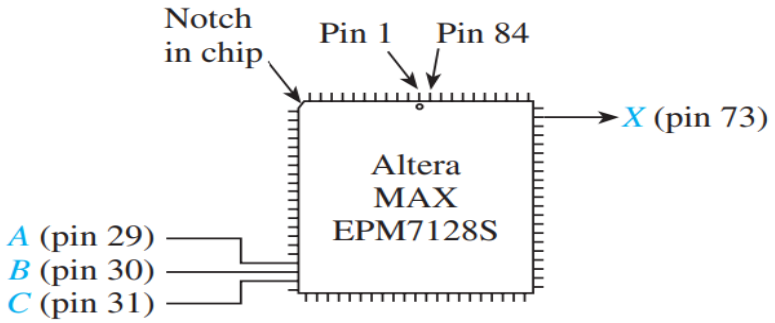


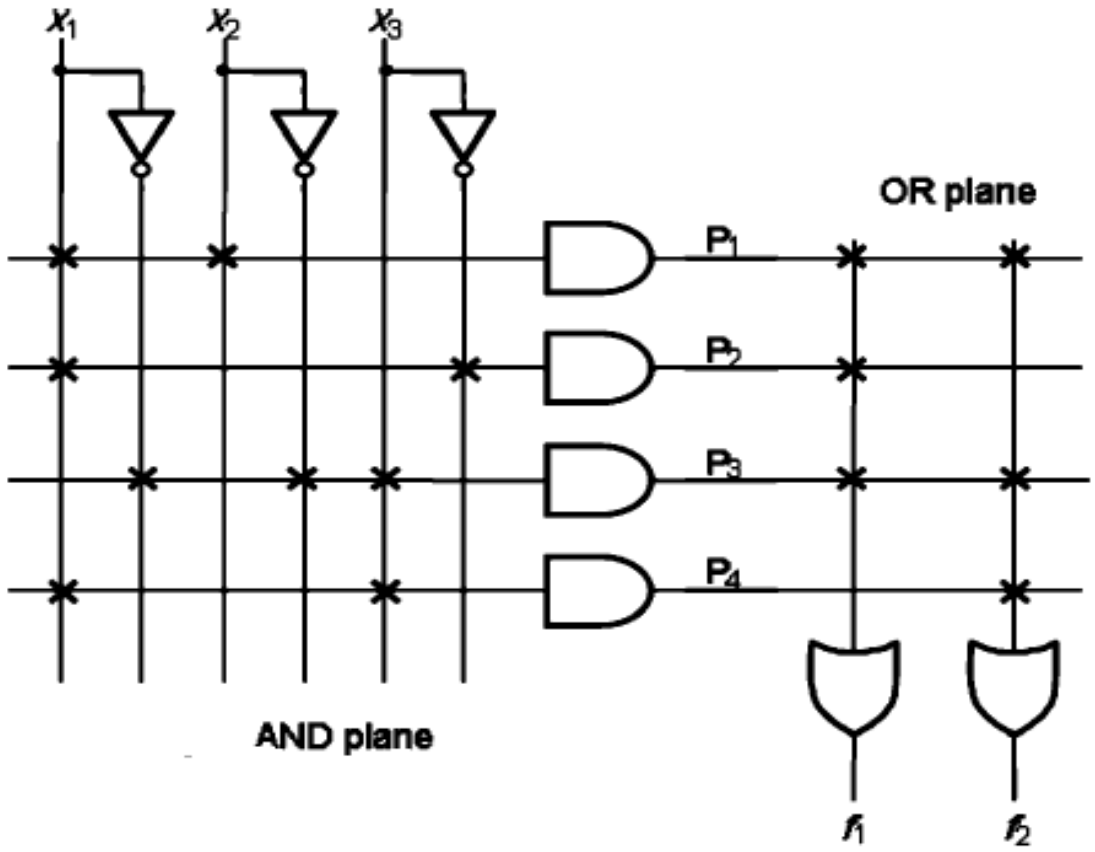
Figure 2 Implementing the equation $X = \overline{A}B + \overline{B + C}$ using a PLD.

EXAMPLE: Design the following functions by using PLA type of SPLDs

f1 = x1x2+x1x3'+x1'x2'x3

f2 = x1x2+x1'x2'x3+x1x3

SOLUTION:



EXAMPLE : Implement X, Y and Z with PLA of equations below

P1 = $\overline{A}\,\overline{C}$

P2 = $\overline{A}\,C$

P3 = $A\,\overline{B}$

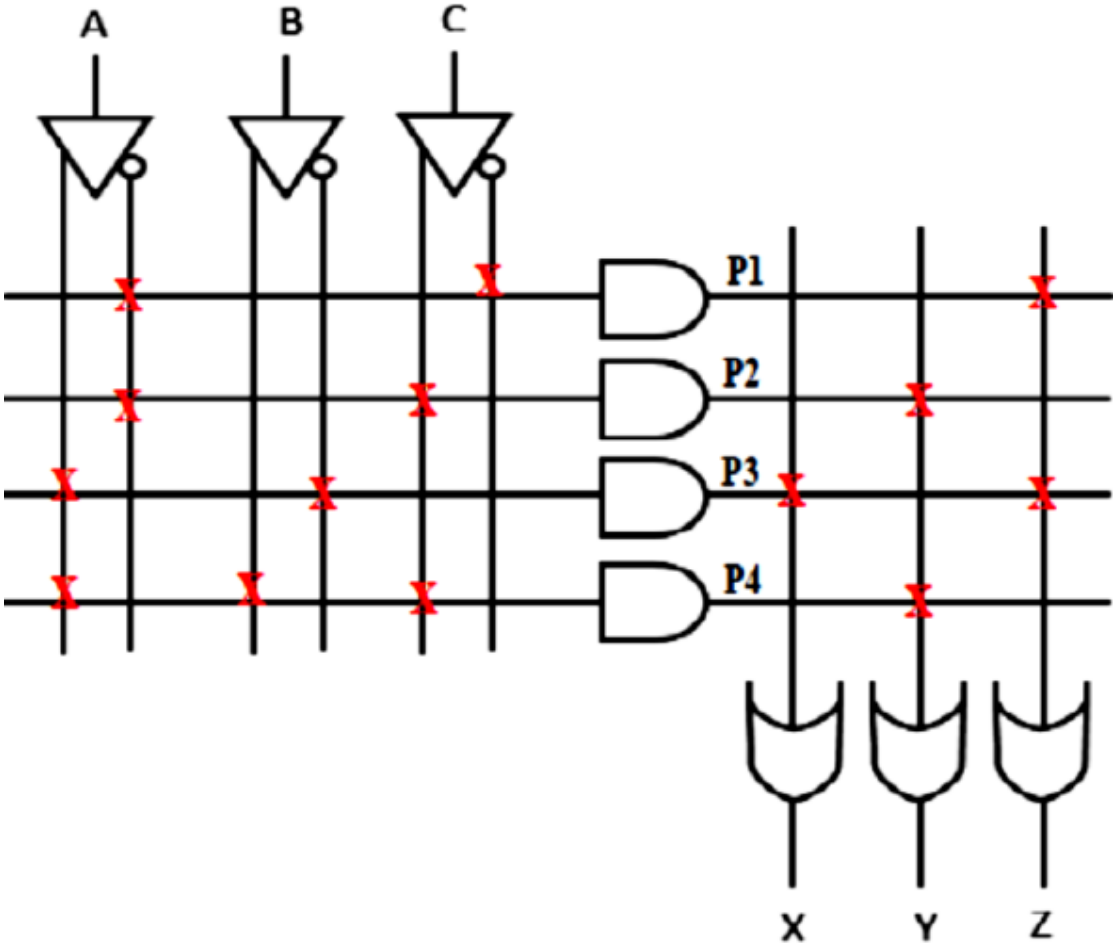
P4 = A B C

X = P3

Y = P2 + P4

Z = P1 + P3

SOLUTION:

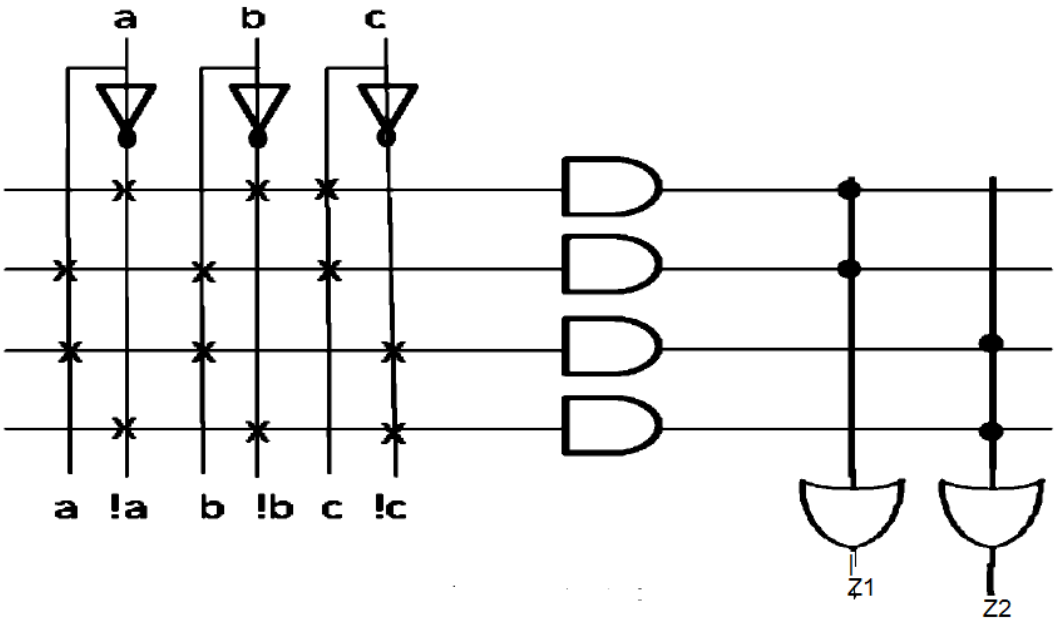


EXAMPLE:

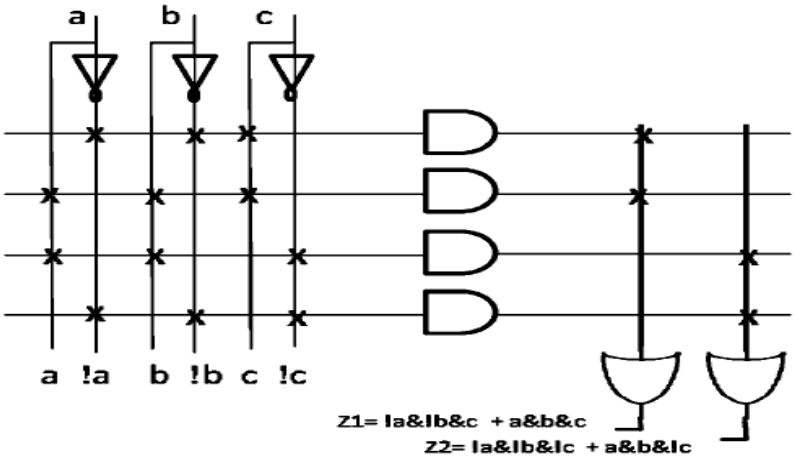
By using PROM,PLA and PAL +execute the functions below

Z1 = !a&!b&c + a&b&c

Z2= !a&!c&!b + a&b&!c SOLUTION: BY USING **PAL**.

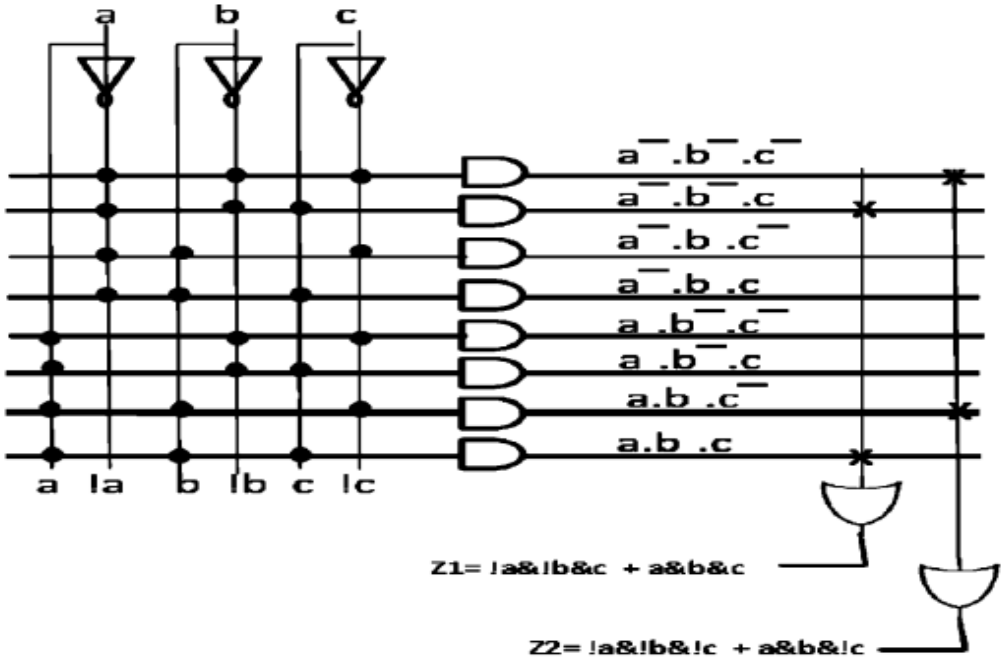


BY USING **PLA**



Programmable Read-Only Memory(PROM)

BY USING PROM

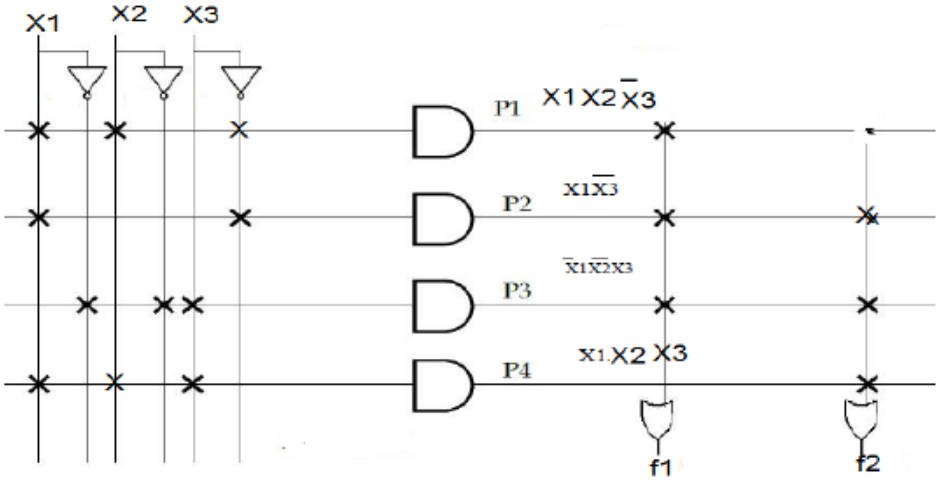


Example

Plot the **PLA** for the two output functions as if both in one device

f1 (x1,x2,x3) =X1X2$\overline{X}$3+X1$\overline{X}$3+$\overline{X}$1$\overline{X}$2X3

f2 (x1,x2,x3) =X1$\overline{X}$3+$\overline{X}$1$\overline{X}$2X3+X1X2X3



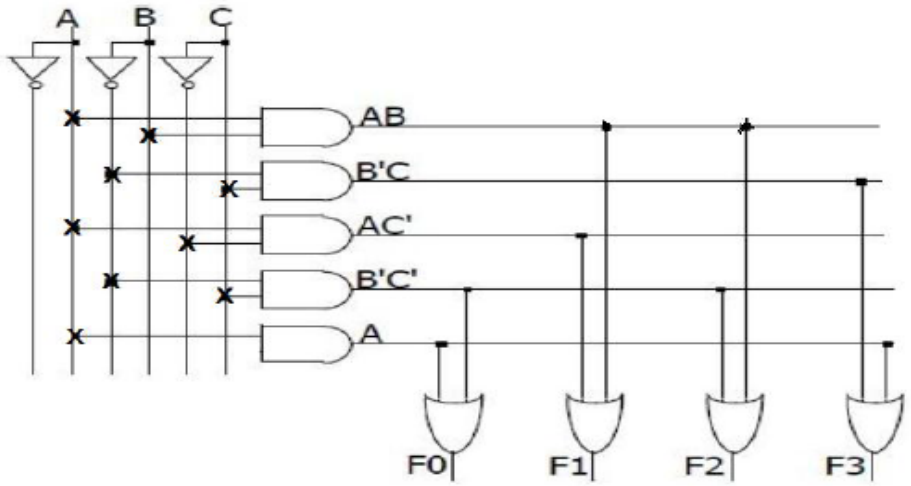
EXAMPLE: Design the following functions by using PAL type of SPLDs

F0=A+!B!C

F1=A!C+AB

F2=!B!C+AB

F3=A+!BC

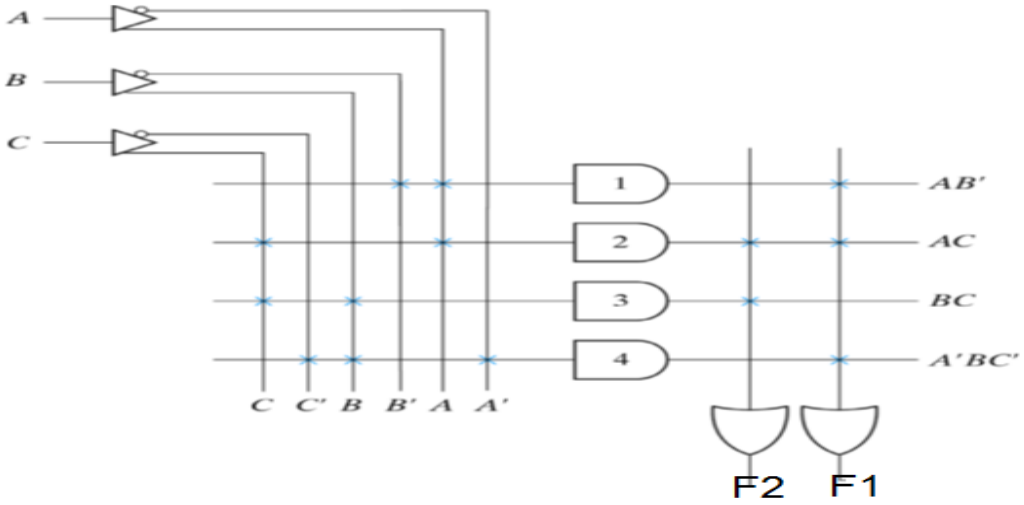


EXAMPLE : PLA with 3 inputs and two outputs ?

F1=$A\overline{B} + AC + \overline{A}B\overline{C}$

F2=$AC + BC$

SOLUTION:



Example: implement the following function using suitable PLA device.

F1 = A B C

F2 = A + B + C

F3 = A' B' C'

F4 = A' + B' + C'

F5 = A xor B xor C

F6 = (A xnor B xnor C)'

A	B	C	F1	F2	F3	F4	F5	F6
0	0	0	0	0	1	1	0	0
0	0	1	0	1	0	1	1	1
0	1	0	0	1	0	1	1	1
0	1	1	0	1	0	1	0	0
1	0	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0	0
1	1	0	0	1	0	1	0	0
1	1	1	1	1	0	0	1	1