Computer Science Dept.

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OUTLINE

- ✓ *Instruction Set of 8086µP*

Instruction Set of 8086μP

Ex : Write an ALP to evaluate x(y + z) where x = 10H, y = 20H and z = 30H and store the result in a memory location 54000H.

```
MOV AX , 5000H
MOV DS , AX
MOV AL , 20H
MOV CL , 30H
ADD AL , CL
MOV CL , 10H
MUL CL
MOV SI , 4000H
MOV [SI] , AX
HLT
```

Instruction Set of 8086µP

Ex: Write an ALP to multiply the word 1234H by the double word 12345678H. Store the result in locations starting in 54000H.

```
MOV AX , 1234H          MOV BX , 5678H
MOV CX , 1234H          MUL BX
MOV SI , AX             MOV DI , DX
MOV AX , 1234H          MUL CX
ADC AX , DI             ADC DX , 0000H
MOV BX , 5000H          MOV DS , BX
MOV [4000H], SI         MOV [4002H],AX
MOV [4004H],DX          HLT
```

Instruction Set of 8086μP

Note: After executing **AND** , **OR**, or **XOR** instructions CF and OF are both 0. PF, SF, and ZF are updated . AF is undefined.

Ex : Write an ALP to clear bits 0 to 5, set bits 6 to 10 and complement bits 11 to 15 in a memory location 34000H.

Ans.

MOV AX , 3000H

MOV DS , AX

AND [4000] , FFC0H

OR [4000] , 07C0H

XOR [4000] , F800H

HLT

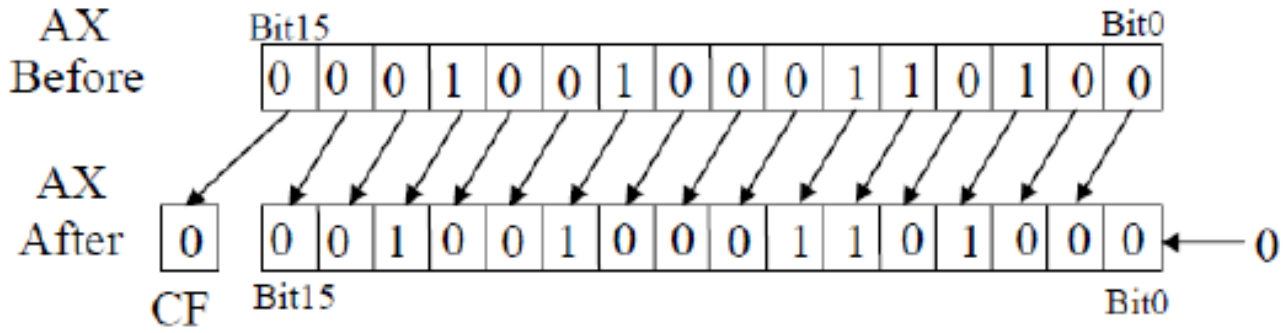
Instruction Set of 8086μP

Shift Instructions:

Shift instructions can perform two basic types of shift operations: **the logical shift** and **the arithmetic shift**. Also, each of these operations can be performed to the right or to the left. They have the ability to shift the contents of either an internal register or a storage location in memory.

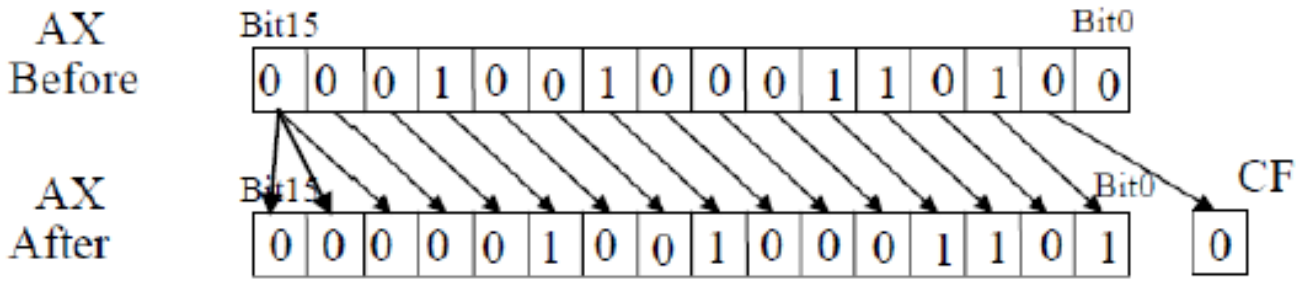
Instruction Set of 8086μP

Ex: If (AX)=1234H , then, executing: SHL AX , 1



(AX) = 2468H & (CF)=0

Ex: If (CL)=2 and (AX)= 1234AH. Then, executing: SAR AX , CL leads to:
(AX)=048EH & (CF)=0

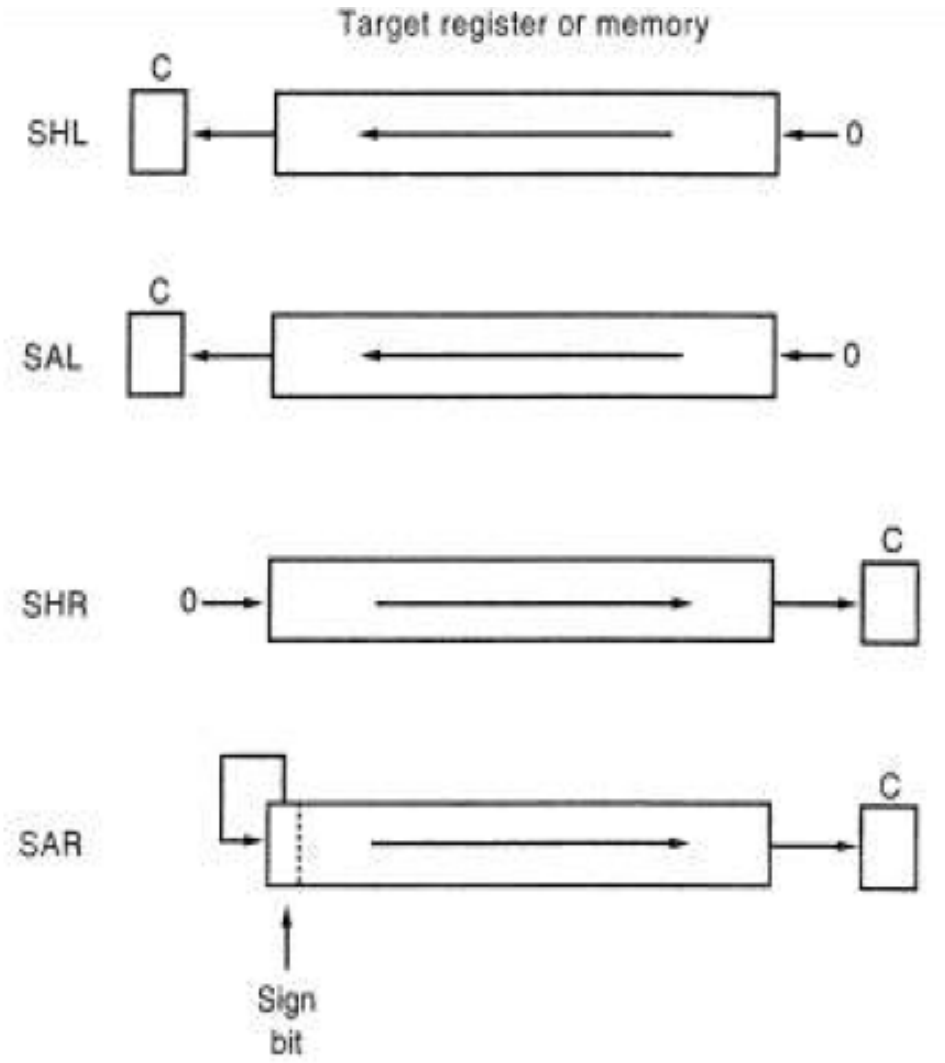


Instruction Set of 8086μP

Mnemonic	Meaning	Format	Operation	Flags affected
SAL/SHL	Shift arithmetic left / Shift logical left	SHL D , 1 SHL D , CL SAL D , 1 SAL D , CL	Shift D (Reg. / Mem.) to left either by 1 bit or by number of bits stored in CL .	CF, PF, SF, Z AF undefined OF undefined if count ≠1
SHR	Shift logical right	SHR D , 1 SHR D , CL	Shift D (Reg. / Mem.) to right either by 1 bit or by number of bits stored in CL .	CF, PF, SF, Z AF undefined OF undefined if count ≠1
SAR	Shift arithmetic right	SAR D , 1 SAR D , CL	Shift D (Reg. / Mem.) either by 1 bit or by number of bits stored in CL .	CF, PF, SF, Z AF undefined OF undefined if count ≠1

Instruction Set of 8086μP

- **Logical Shift**
  - Left SHL
  - Right SHR
- **Arithmetic Shift**
  - Left SAL
  - Right SAR



Instruction Set of 8086μP

Rotate (ROL, ROR, RCL, and, RCR) Instructions:

Rotate instructions, are similar to the shift instructions. The operation of these instructions is described below. They have the ability to rotate the contents of either an internal register or a storage location in memory.

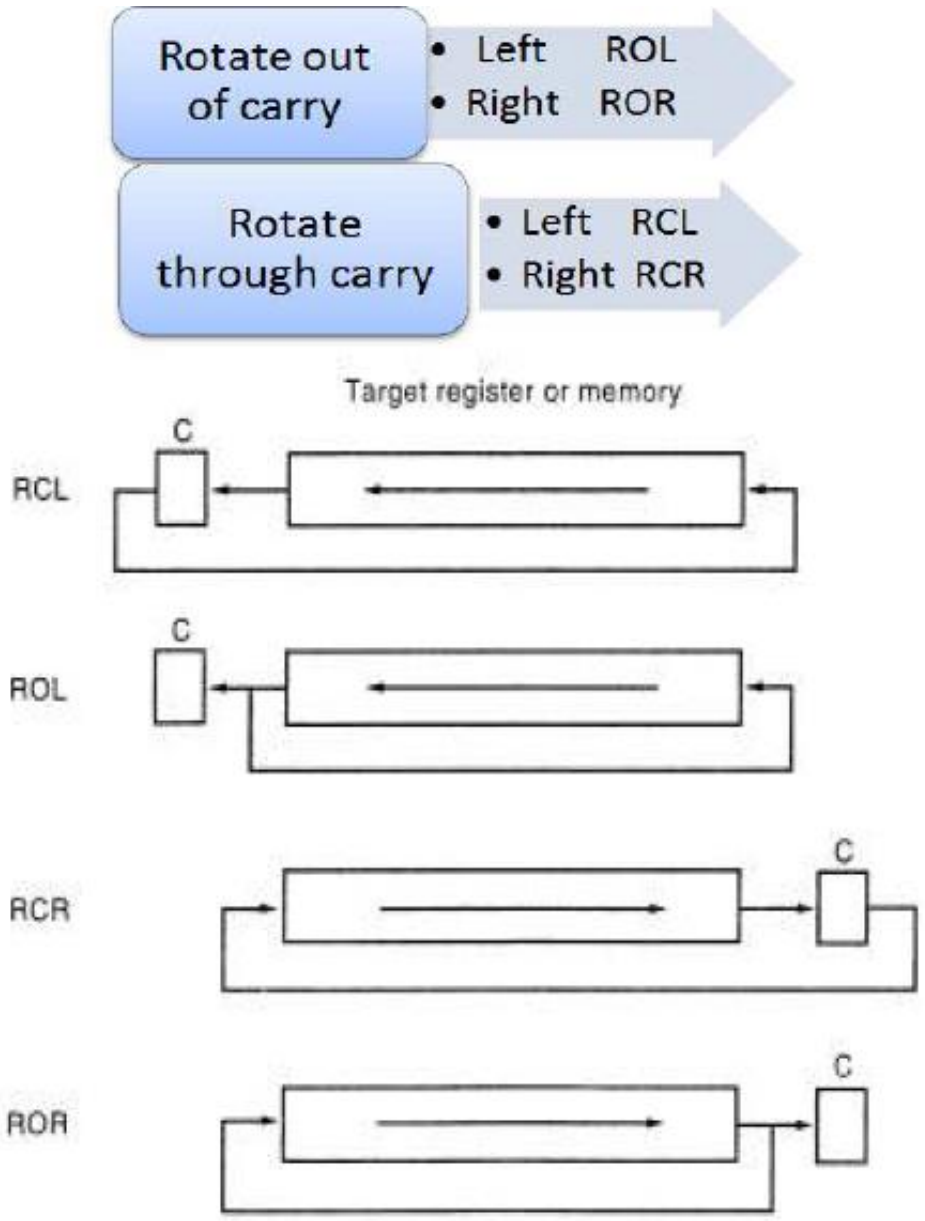
Mnemonic	Meaning	Format	Operation	Flags affected
ROL	Rotate left	ROL D , 1 ROL D , CL	Rotate D (Reg./Mem.) left out of carry either by 1 bit or No. of bits stored in CL .	CF OF undefined if count ≠1
ROR	Rotate right	ROR D , 1 ROR D , CL	Rotate D (Reg./Mem.) right out of carry either by 1 bit or No. of bits stored in CL .	CF OF undefined if count ≠1
RCL	Rotate left through carry	RCL D , 1 RCL D , CL	Rotate D (Reg./Mem.) left through carry either by 1 bit or No. of bits in CL .	CF OF undefined if count ≠1
RCR	Rotate right through carry	RCR D , 1 RCR D , CL	The same operation of RCL but to the right.	CF OF undefined if count ≠1

Instruction Set of 8086μP

Rotate (ROL, ROR, RCL, and, RCR) Instructions:

Rotate instructions, are similar to the shift instructions. The operation of these instructions is described below. They have the ability to rotate the contents of either an internal register or a storage location in memory.

Instruction Set of 8086μP



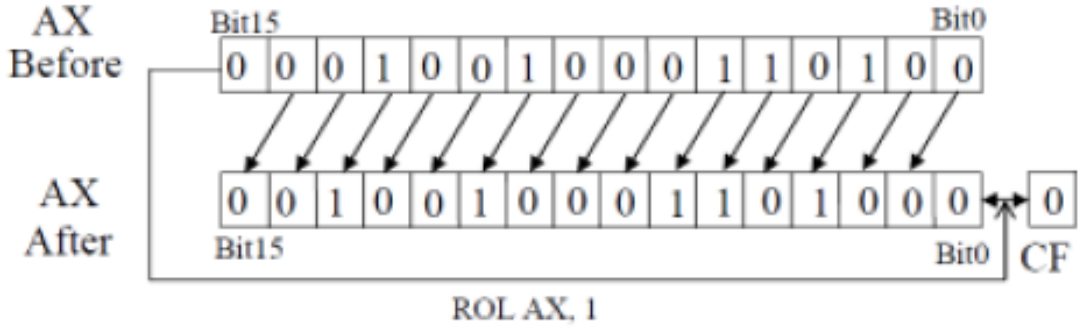
Instruction Set of 8086μP

Ex : If (CL) =04_{16} and AX=$1234A_{16}$. Determine the new contents of AX and the carry flag after executing the instructions:

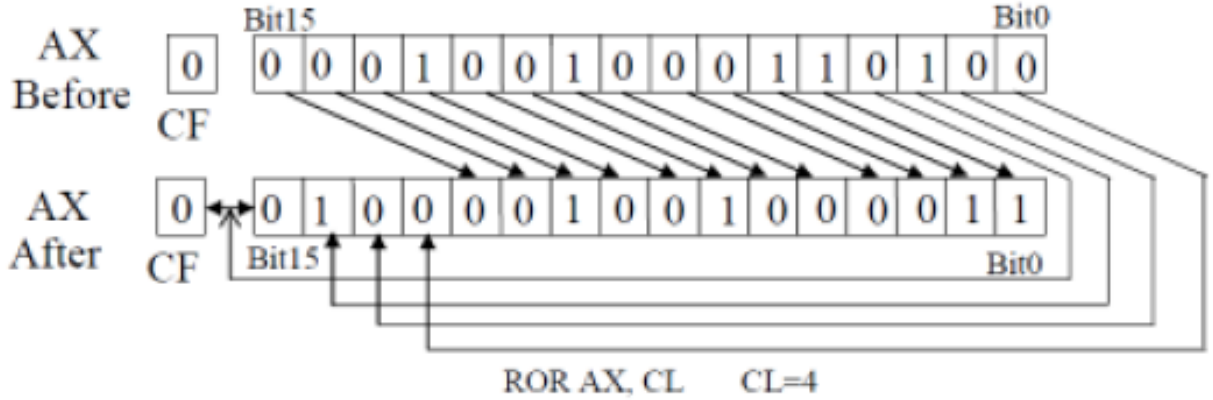
a) ROL AX, 1 b) ROR AX, CL

Ans.

a) (AX) = 2468H and (CF) = 0



b) (AX) = 4123H and (CF)=1



Instruction Set of 8086μP

Flags Control Instructions

The flag control instruction affect the state of the flags directly, these instructions and their operation are listed below:

Mnemonic	Meaning	Operation	Flags affected
LAHF	Load AH from flags	(AH)←(Flags)	None
SAHF	Store AH into flags	(Flags)←(AH)	SF,ZF,AF,PF,CF

LAHF instruction : Load (copy to) AH with the low byte the flag register.

(AH) ← (Low byte of flag register)

SAHF instruction Store (copy) AH register to low byte of flag register.

(Low byte of flag register) ← (AH)

Instruction Set of 8086μP

Ex: Write an ALP that complements the first byte of flags register.

LAHF

XOR AH , 0FFH

SAHF

HLT

Mnemonic	Meaning	Operation	Flags affected
CLC	Clear carry flag	(CF)←0	CF
STC	Set carry flag	(CF)←1	CF
CMC	Complement carry flag	(CF)←NOT (CF)	CF
CLI	Clear interrupt flag	(IF)←0	IF
STI	Set interrupt flag	(IF)←1	IF

Mnemonic	Meaning	Format	Operation	Flags affected
CLD	Clear DF	CLD	(DF)←0	DF
STD	Set DF	STD	(DF)←1	DF

Instruction Set of 8086μP

Compare CMP and TEST Instructions

The following are the characteristics of CMP instruction:

- Can compare two 8-bit or two 16-bit numbers.
- Operands many reside in memory, a register in the CPU or be a part of an instruction.
- CMP is a subtraction method, it uses 2's complement .
- Result of CMP is not saved in the destination operand.
- Results of comparison is reflected in the six status flags: CF, AF, OF, PF, SF and ZF.

Mnemonic	Meaning	Format	Operation	Flags affected
CMP	Compare	CMP D, S	(D)-(S) is used in setting or resetting the flags	CF, AF, OF, PF, SF, ZF

Instruction Set of 8086μP

Destination	Source
Register	Register
Register	Memory
Memory	Register
Register	Immediate
Memory	Immediate
Accumulator	Immediate

Examples

CMP AX , BX
CMP DL , CL
CMP AL , [BX]
CMP CX , 1234h
CMP [SI+100H] , 1234H

$CMP\ AX\ ,BX$

$AX > BX \rightarrow CF = 0$
$AX < BX \rightarrow CF = 1$
$AX = BX \rightarrow ZF = 1$

Instruction Set of 8086μP

The TEST Instruction

This instruction ANDs the contents of a source byte or word with the contents of specified destination word. Flags are updated but neither operand is changed. TEST instruction is often used to set flags before a conditional jump instruction.

Mnemonic	Meaning	Format	Operation	Flags Affected
TEST	test	TEST D , S	(D) . (S)	PF , ZF , SF


THANK
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