Chapter Four
Field-Effect Transistors (FET)

- **Introduction:**

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor. Although there are important differences between the two types of devices, there are also many similarities that will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that the BJT transistor is a *current-controlled* device as depicted in Fig.1a, while the JFET transistor is a *voltage-controlled* device as shown in Fig.1b. In other words, the current I_C in Fig.1a is a direct function of the level of I_B. For the FET the current I will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 1b. In each case the current of the output circuit is being controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

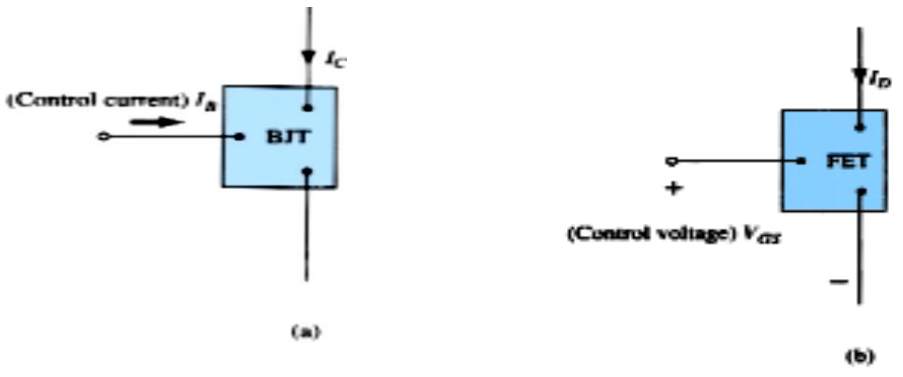


Figure 1

- There are *n-channel* and *p-channel* field-effect transistors
- Two types of FETs will be introduced: the *junction field-effect transistor* (JFET) and the *metal-oxide-semiconductor field-effect transistor (MOSFET).*

- **CONSTRUCTION AND CHARACTERISTICS OF JFETS:**

The basic construction of the *n*-channel JFET is shown in Fig. 2. Note that the major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D),* while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).* The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p*-*n* junctions under no-bias conditions.

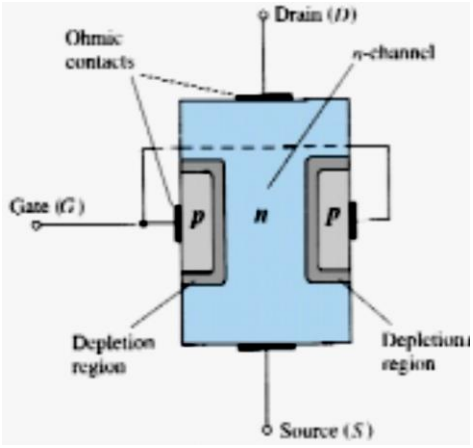


Figure 2

In Fig. 3, a positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition V_{GS} = 0 V. As the voltage V_{DS} is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear. If V_{DS} is increased to a level where it appears that the two depletion regions would "touch", a condition referred to as *pinch-off* will result.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions V_{GS} = 0 V and $V_{DS} > |V_p|$.

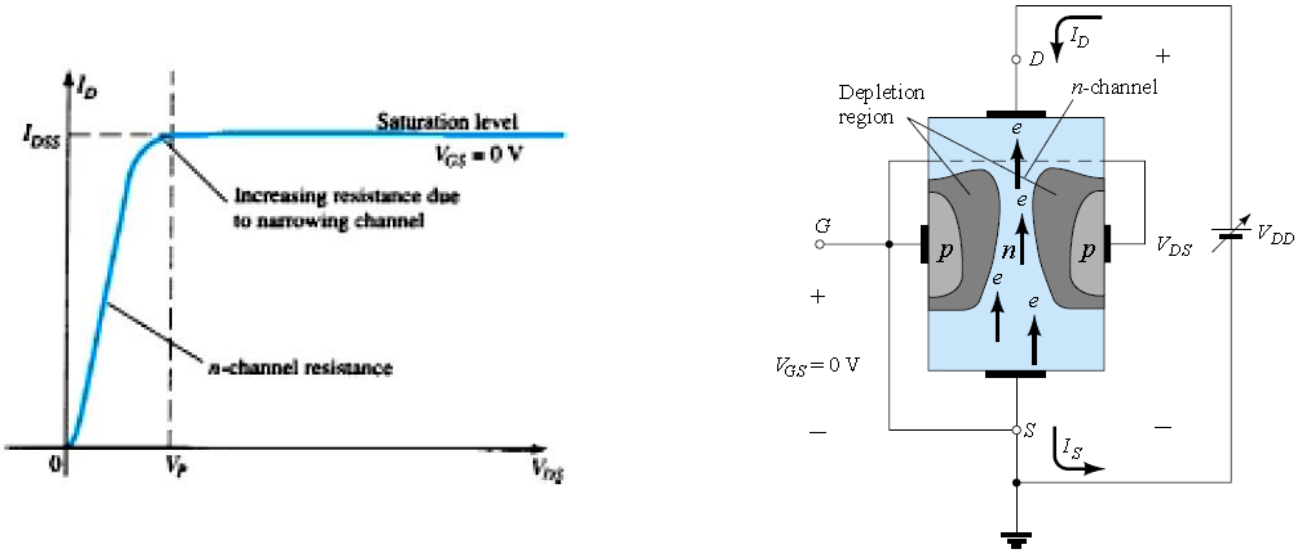


Figure 3

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. Note also on Fig. 4 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = V_p$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off."

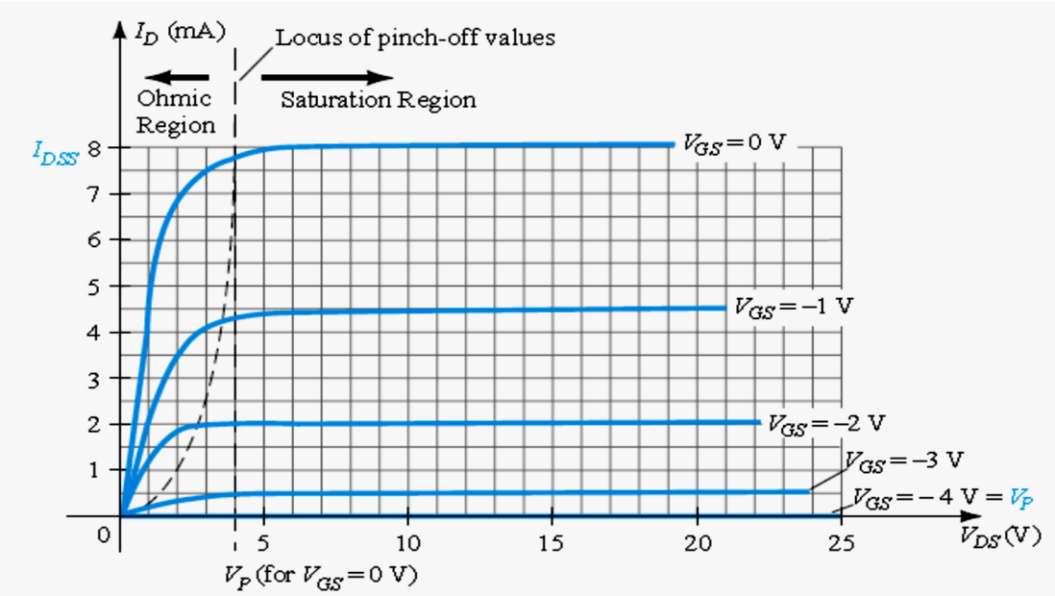


Figure 4: *n*-Channel JFET characteristics with I_{DSS} = 8 mA and V_p= - 4 V.

The level of V_{GS} that results in I_D = 0 mA is defined by $V_{GS} = V_p$, with V_p being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

- **Voltage-Controlled Resistor:**

The region to the left of the pinch-off locus of Fig. 4 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

where r_0 is the resistance with V_{GS} = 0 V and r_d the resistance at a particular level of V_{GS}. For example, if *n*-channel JFET with r_o equal to 10 kΩ (V_{GS} = 0 V), V_p =- 6 V, will result in 40 kΩ at V_{GS} = -3 V.

- ***p*-Channel Devices:**

The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 3, but with a reversal of the *p*- and *n*-type materials as shown in Fig. 5.

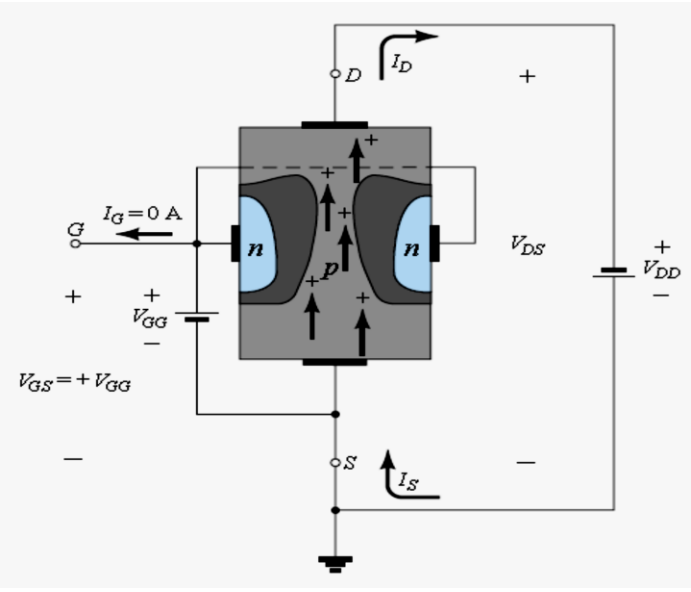


Figure 5

The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 6.

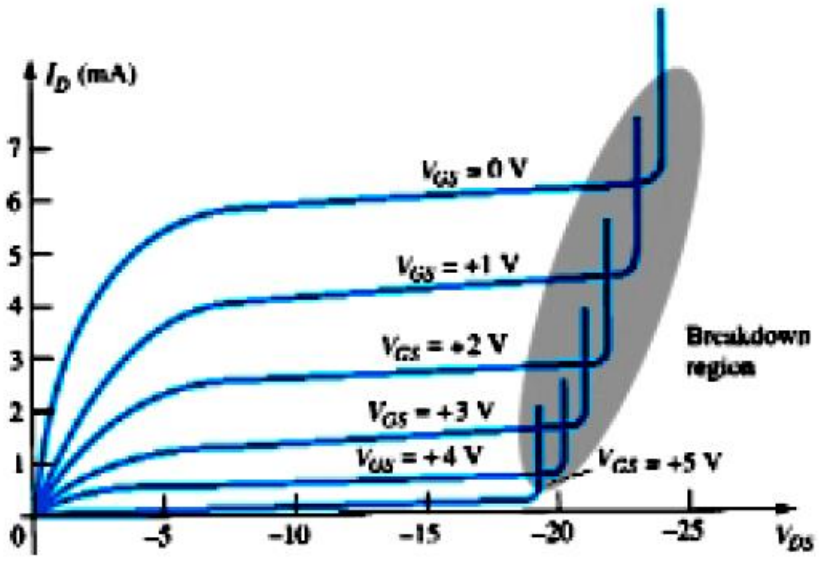


Figure 6: *p*-Channel JFET characteristics with I_{DSS} = 6 mA and V_p = +6 V.

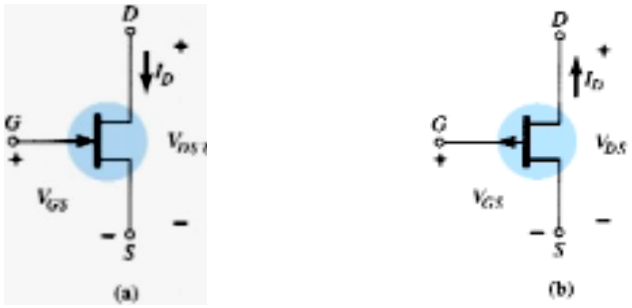
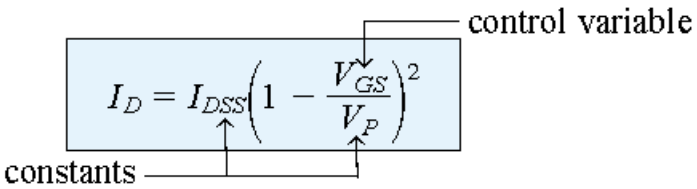


Figure 7: JFET symbols: (a) *n*-channel; (b) *p*-channel.

- **TRANSFER CHARACTERISTICS:**

The relationship between I_D and V_{GS} is defined by *Shockley'equation:*



The squared term of the equation will result in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

By using basic algebra we can obtain an equation for the resulting level of V_{GS} for a given level of I_D.

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

In Fig.8 two graphs are provided, with the vertical scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS}, while the other is I_D versus V_{GS}.

In review:

When V_{GS} = 0 V, $I_D = I_{DSS}$, and when $V_{GS} = V_P$, I_D = 0 mA.

The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$P_D = V_{DS}\, I_D$$

- **IMPORTANT RELATIONSHIPS:**

JFET		***BJT***
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

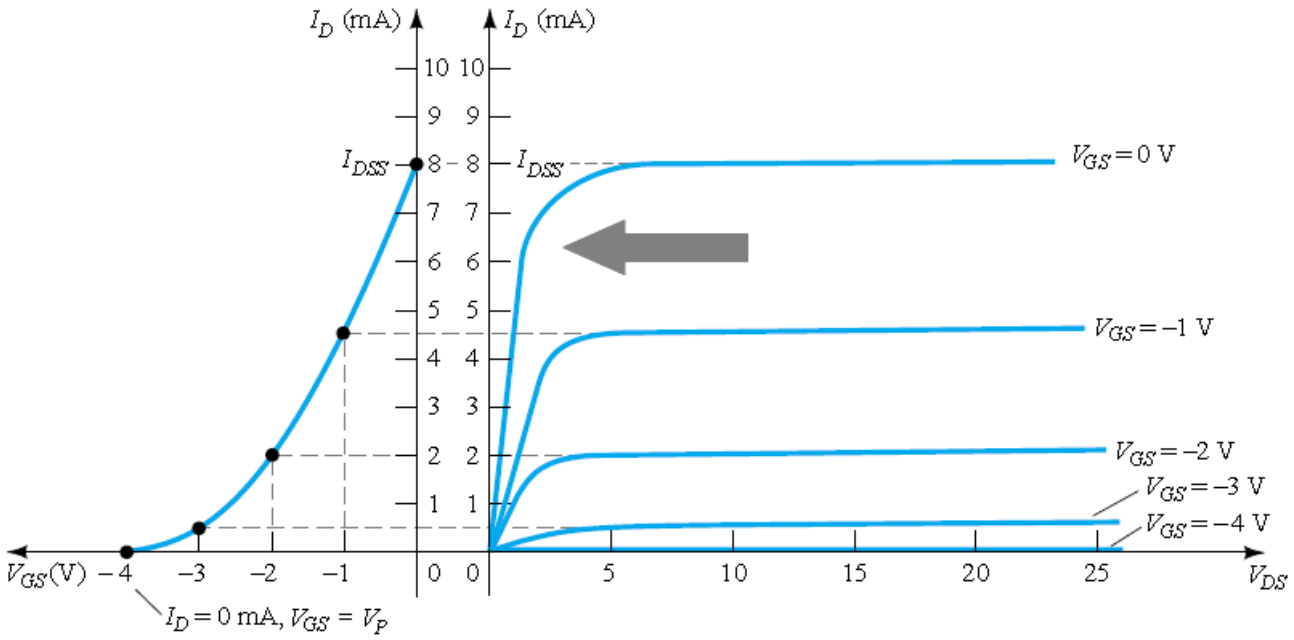


Figure 8

- **FET Biasing:**

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \approx 0 \text{ A} \qquad \text{and} \qquad I_D = I_S$$

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 9. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach.

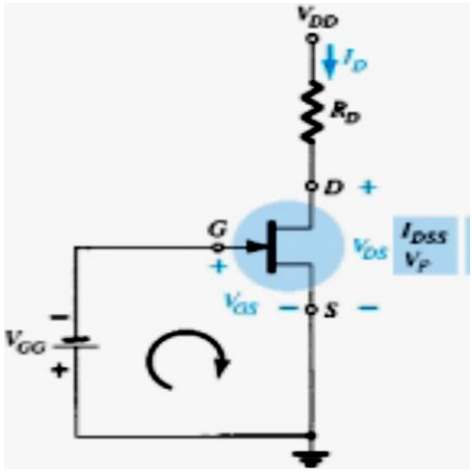


Figure 9

$I_G = 0$ A and $V_{RG} = I_G R_G = (0 \text{ A})R_G = 0$ V

Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig.9 will result in

$$-V_{GG} - V_{GS} = 0 \quad and \quad V_{GS} = -V_{GG}$$

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0 \quad and \; V_{DS} = V_{DD} - I_D R_D$$

For the configuration of Fig. 9,

$$V_S = 0$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S \;\; or \;\; V_D = V_{DS} + V_S = V_{DS} + 0V \;\; and \;\; V_D = V_{DS}$$

In addition, $V_{GS} = V_G - V_S \;\; or \; V_G = V_{GS} + V_S = V_{GS} + 0V \; and \; V_G = V_{GS}$

Example 1: Determine the following for the network of Fig. 10.

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.

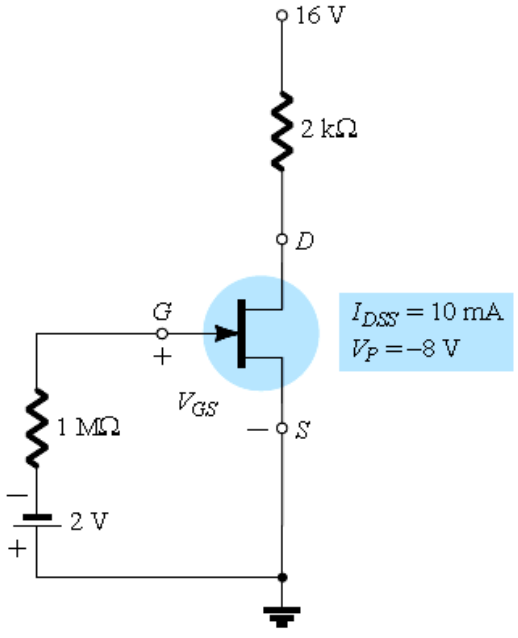


Figure 10

Mathematical Approach:

(a) $V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$

(b) $I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\ \text{mA}\left(1 - \frac{-2\ \text{V}}{-8\ \text{V}}\right)^2$

$= 10\ \text{mA}(1 - 0.25)^2 = 10\ \text{mA}(0.75)^2 = 10\ \text{mA}(0.5625)$

$= \mathbf{5.625\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.625\ \text{mA})(2\ \text{k}\Omega)$

$= 16\ \text{V} - 11.25\ \text{V} = \mathbf{4.75\ V}$

(d) $V_D = V_{DS} = \mathbf{4.75\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

Graphical Approach:

Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve. The resulting Shockley curve and the vertical line at V_{GS} = -2 V are provided in Fig.11

$$V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{DQ} = \mathbf{5.6\ mA}$

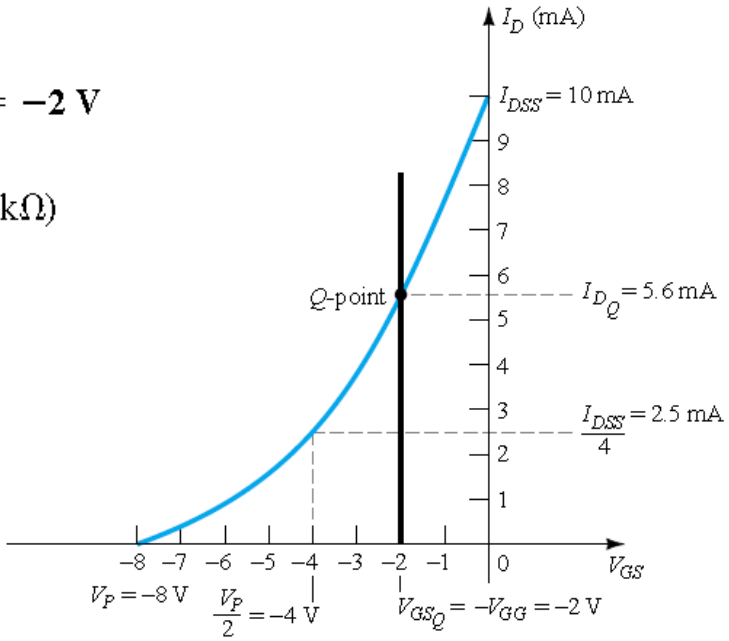
(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$

$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

(d) $V_D = V_{DS} = \mathbf{4.8\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$



The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

-SELF-BIAS CONFIGURATION:

$V_{R_s} = I_D R_S$

The current through R_S is the source current I_S , but $I_S = I_D$ and

$$-V_{GS} - V_{R_s} = 0$$

and

$$V_{GS} = -V_{R_s}$$

or

$$\boxed{V_{GS} = -I_D R_S}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

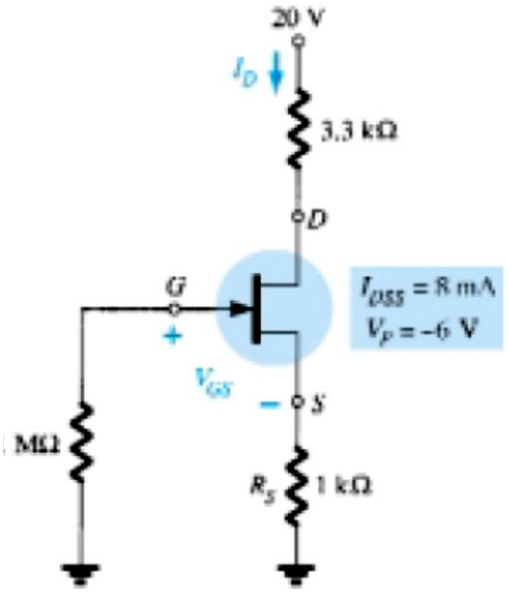
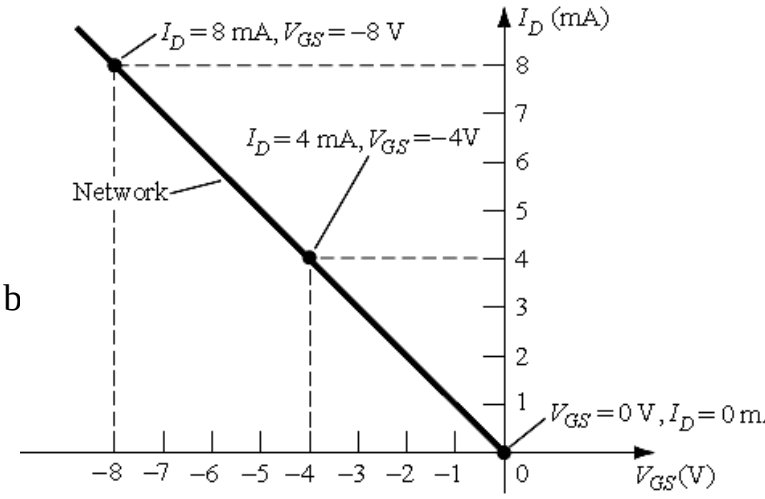


Figure 11

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

Example 2: Determine the following for the network of Fig. 11.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_S.
(e) V_G.
(f) V_D.



(a) The gate-to-source voltage is determined b

$V_{GS} = -I_D R_S$

Choosing $I_D = -4mA$ obtained $V_{GS} = -4V$

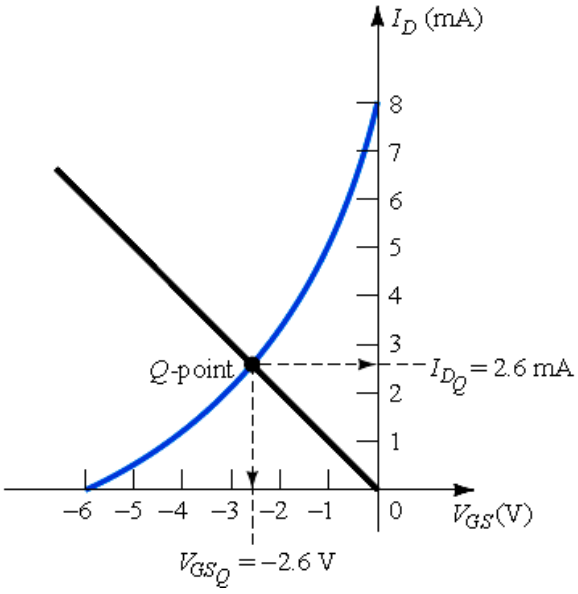
And plot the line as shown.

For Shockley's equation, if we choose

$V_{GS} = V_P/2 = -3V$ *then* $I_D = I_{DSS}/4 = 2mA$

And plot of fig. below will represent the characteristic of the device

from the plot we obtain V_{GSQ} =- **2.6 V**



(b) At the quiescent point:
I_{DQ} = **2.6 mA**

(c) $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega)$
$= 20\text{ V} - 11.18\text{ V}$
$= \mathbf{8.82\text{ V}}$

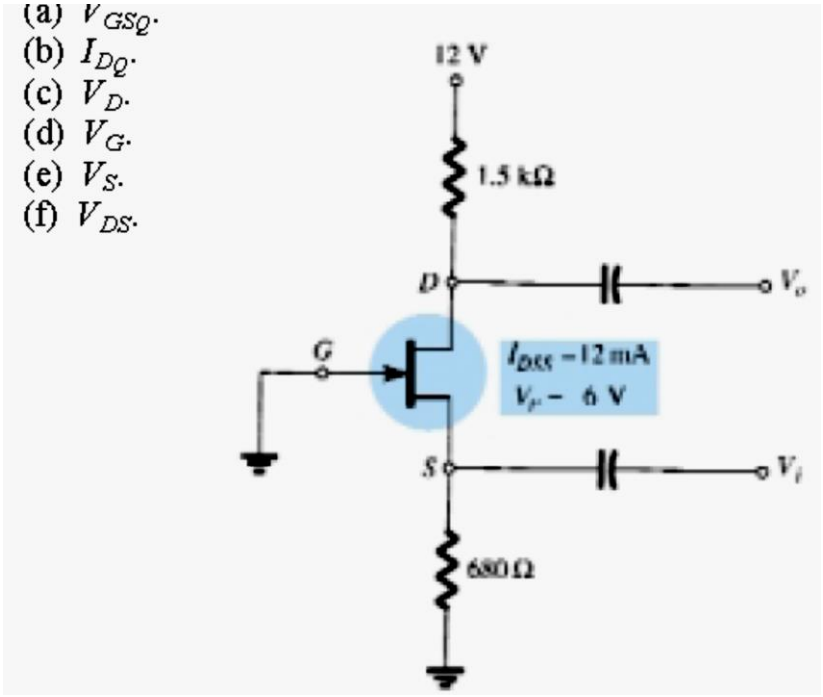
(d) $V_S = I_D R_S$
$= (2.6\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.6\text{ V}}$

(e) $V_G = 0$

(f) $V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\text{ V}}$
$V_D = V_{DD} - I_D R_D = 20\text{ V} - (2.6\text{ mA})(3.3\text{ k}\Omega) = \mathbf{11.42\text{ V}}$

Home work: Determine the following for the common-gate configuration of Fig.

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_D.
(d) V_G.
(e) V_S.
(f) V_{DS}.



VOLTAGE-DIVIDER BIASING:

The network of Fig. 12 is redrawn as shown in Fig. 13 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent.

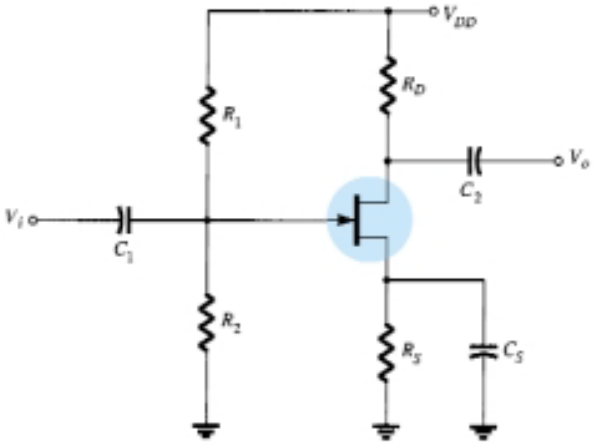


Figure 12

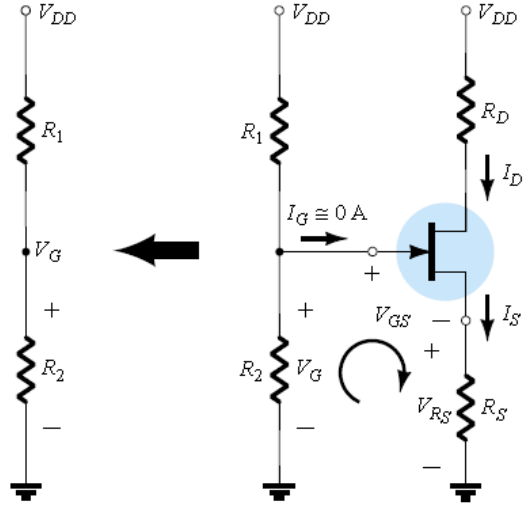


Figure 13

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig.13 will result in

$$V_G - V_{GS} - V_{RS} = 0$$

and

$$V_{GS} = V_G - V_{RS}$$

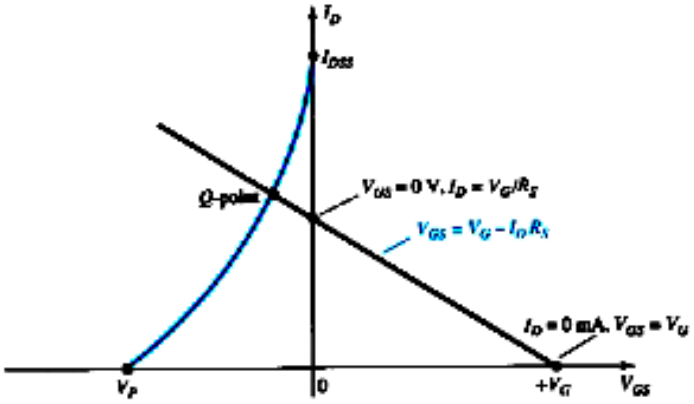
Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S$$

If we *select* I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting I_D = 0 mA and finding the resulting value of V_{GS} as follows:

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\text{ mA})R_S$$

$$\boxed{V_{GS} = V_G\big|_{I_D = 0\text{ mA}}}$$



For the other point, let us now employ the fact that at any point on the vertical axis V_{GS} =0 V and solve for the resulting value of I_D:

$$V_{GS} = V_G - I_D R_S$$
$$0\text{ V} = V_G - I_D R_S$$

$$\boxed{I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0\text{ V}}}$$

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.

The remaining network analysis can be performed in the usual manner. That is,

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

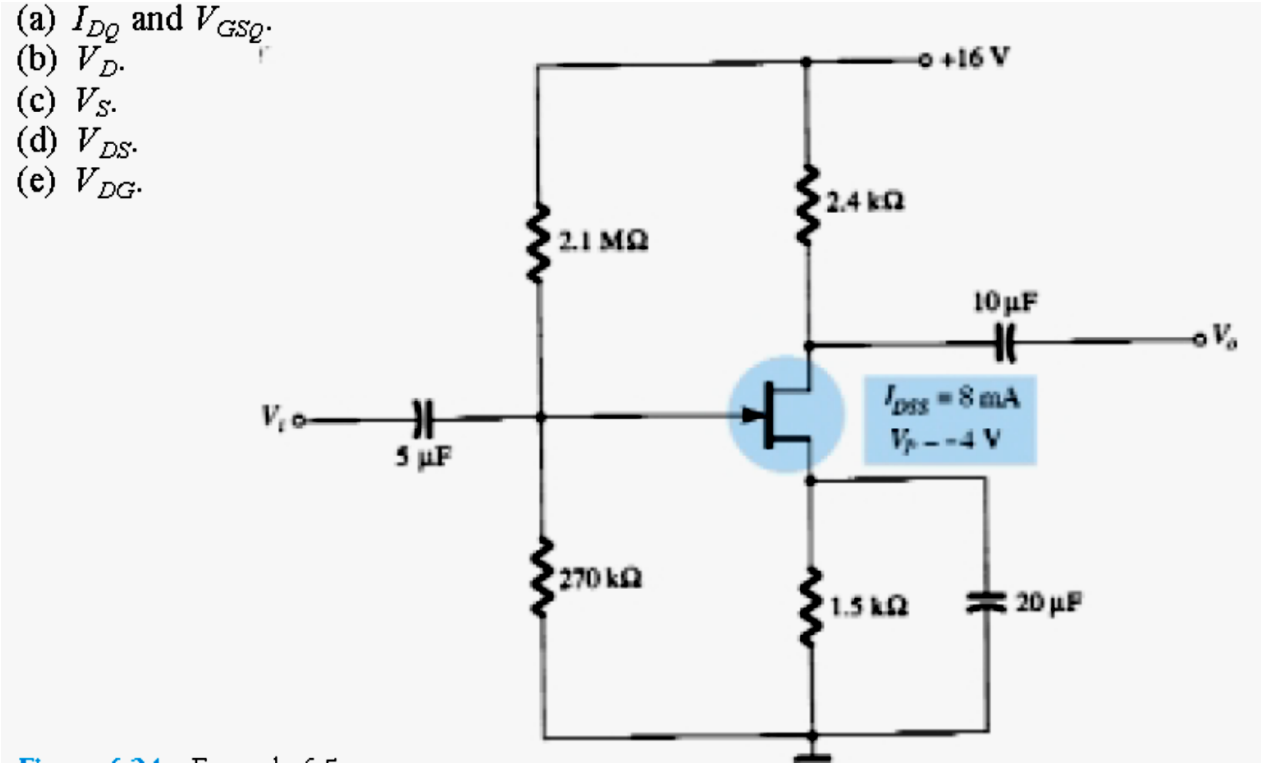
$$\boxed{V_D = V_{DD} - I_D R_D}$$

$$\boxed{V_S = I_D R_S}$$

$$\boxed{I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}}$$

Example: Determine the following for the network of Fig. bellow:

(a) I_{DQ} and V_{GSQ}.
(b) V_D.
(c) V_S.
(d) V_{DS}.
(e) V_{DG}.



(a) For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. . The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega}$$

$$= 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\text{ V}$$

When $V_{GS} = 0$ V:

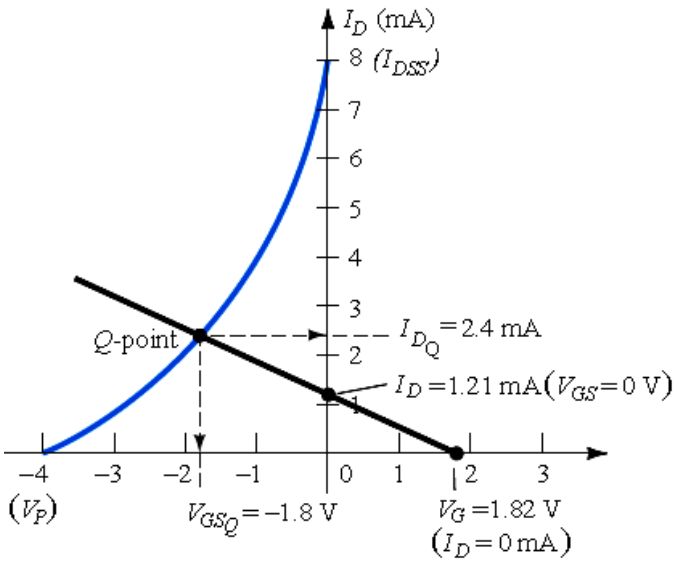
$$I_D = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

The resulting bias line appears on Fig. bellow with quiescent values of

$$I_{DQ} = \mathbf{2.4\text{ mA}}$$

and

$$V_{GSQ} = \mathbf{-1.8\text{ V}}$$



(b) $V_D = V_{DD} - I_D R_D$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega)$

$= \mathbf{10.24\text{ V}}$

(c) $V_S = I_D R_S = (2.4\text{ mA})(1.5\text{ k}\Omega)$

$= \mathbf{3.6\text{ V}}$

(d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega + 1.5\text{ k}\Omega)$

$= \mathbf{6.64\text{ V}}$

or $V_{DS} = V_D - V_S = 10.24\text{ V} - 3.6\text{ V}$

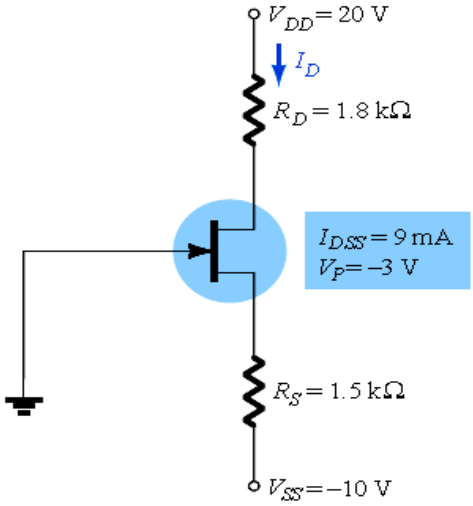
$= \mathbf{6.64\text{ V}}$

(e) Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24\ \text{V} - 1.82\ \text{V}$$
$$= \mathbf{8.42\ V}$$

Home work: Determine the following for the network of this Figure:

(a) I_{DQ} and V_{GSQ}.
(b) V_{DS}.
(c) V_D.
(d) V_S.



- **FET Small-Signal Analysis:**

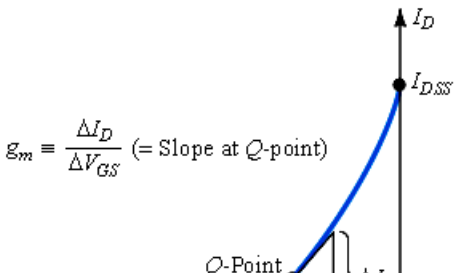
The gate-to-source voltage controls the drain-to-source (channel) current of an FET. The change in collector current that will result from a change in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m\ \Delta V_{GS}$$

Solving for g_m , we have:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

If we now examine the transfer characteristics of Fig. 14, we find that gm is actually the slope of the characteristics at the point of operation. That is,



$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}$$

Figure 14

As V_{GS} approaches 0 V, the magnitude of g_m increases.

Example:

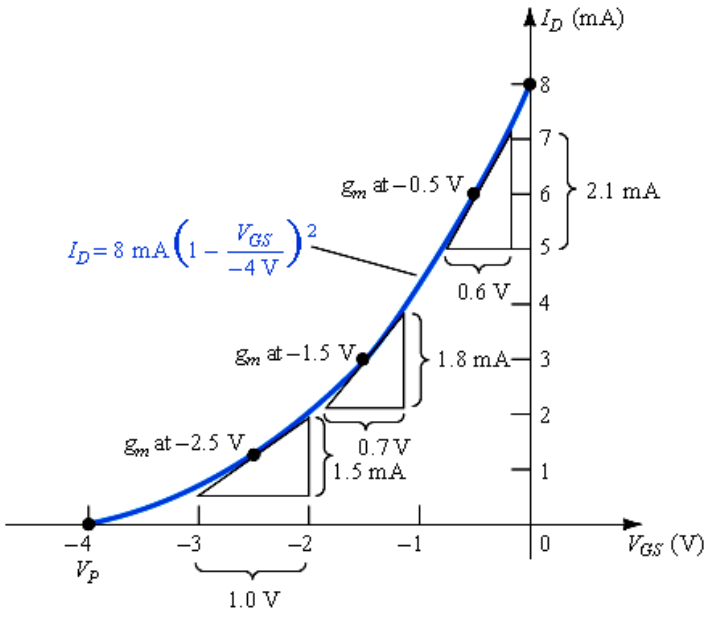
Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at the following dc bias points:
(a) $V_{GS} = -0.5$ V.
(b) $V_{GS} = -1.5$ V.
(c) $V_{GS} = -2.5$ V.

(a) $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\ mS}$

(b) $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\ mS}$

(c) $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\ mS}$

Note the decrease in g_m as V_{GS} approaches V_P.



The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{-pt.}} = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

Where $|V_P|$ denotes magnitude only to ensure a positive value for g_m. The slope of the transfer curve is a maximum at V_{GS} = 0 V. Plugging in V_{GS} = 0 V into above will result in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}}$$

or

$$\boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

Example:

For the JFET having the transfer characteristics of above Example:

(a) Find the maximum value of g_m.

(b) Find the value of g_m at each above operating point and compare with the graphical results.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\ mS}$ (maximum possible value of g_m)

(b) At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\ mS}$$ (versus 3.5 mS graphically)

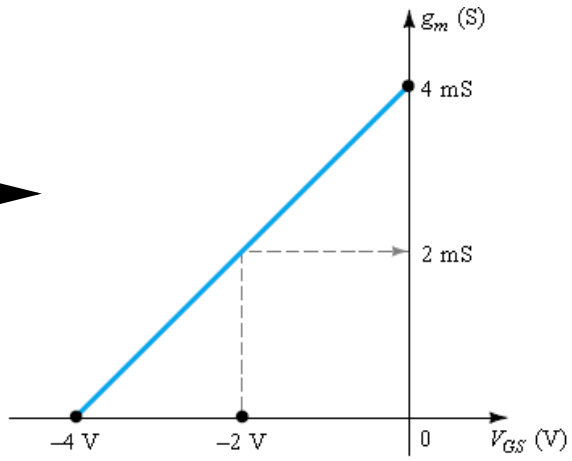
At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\ mS}$$ (versus 2.57 mS graphically)

At $V_{GS} = -2.5$ V,

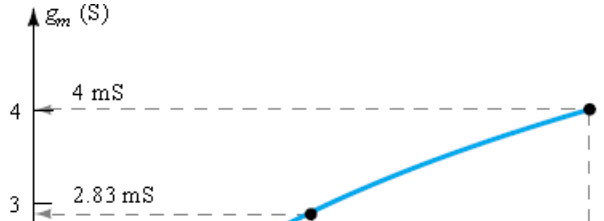
$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\ mS}$$ (versus 1.5 mS graphically)

Plot of g_m vs. V_{GS} for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V.



A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$



Plot of g_m vs. I_D for a JFET with $I_{DSS} = 8$ mA and $V_{GS} = -4$ V.

The plots of clearly reveal that the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D its maximum value of I_{DSS}.

On specification sheets, g_m is provided as y_{fs} where *y* indicates it is part of an admittance equivalent circuit. The *f* signifies *f*orward transfer parameter, and the *s* reveals that it is connected to the source terminal. In equation form,

$$g_m = y_{fs}$$

The input impedance of all commercially available FETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i \text{ (FET)} = \infty\ \Omega$$

The output impedance will typically appear as y_{OS} with the units of μS. The parameter y_{OS} is a component of an *admittance equivalent circuit*, with the subscript *o* signifying an *o*utput network parameter and *s* the terminal (source) to which it is attached in the model.

In equation form,

$$Z_o \text{ (FET)} = r_d = \frac{1}{y_{os}}$$

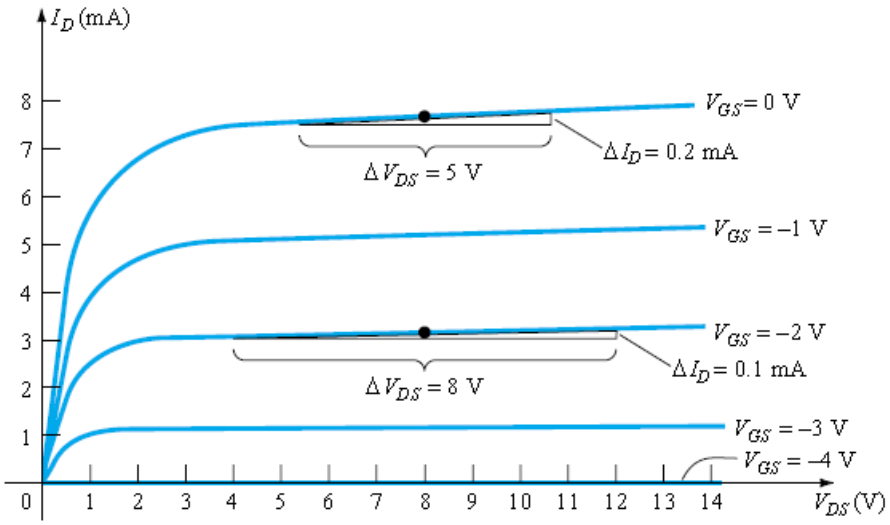
$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

For V_{GS} = 0 V, a tangent line is drawn and ΔV_{DS} is chosen as 5 V, resulting in a ΔI_D of 0.2mA.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = \mathbf{25\ k\Omega}$$

For V_{GS} = -2 V, a tangent line is drawn and ΔV_{DS} is chosen as 8V, resulting in a ΔI_D of 0.1mA.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = \mathbf{80\ k\Omega}$$



- **FET AC Equivalent Circuit**

The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 15. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation. The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source.

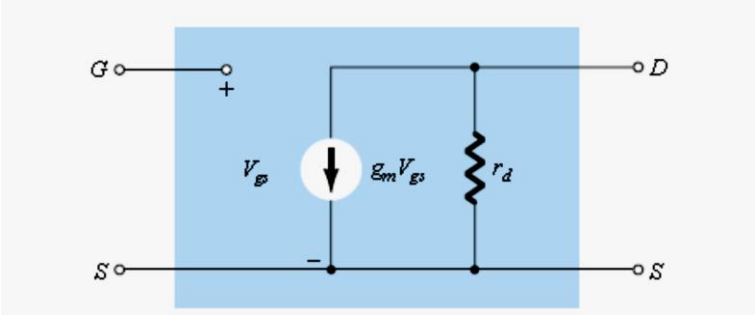


Figure 15

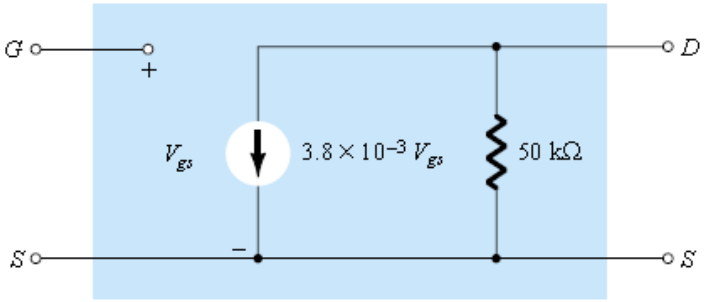
Example;

Given $y_{fs} = 3.8$ mS and $y_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution

$$g_m = y_{fs} = 3.8 \text{ mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

resulting in the ac equivalent model of :



- **fixed-bias**

The *fixed-bias* configuration of Fig.16 includes the coupling capacitors C_1 and C_2 that isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

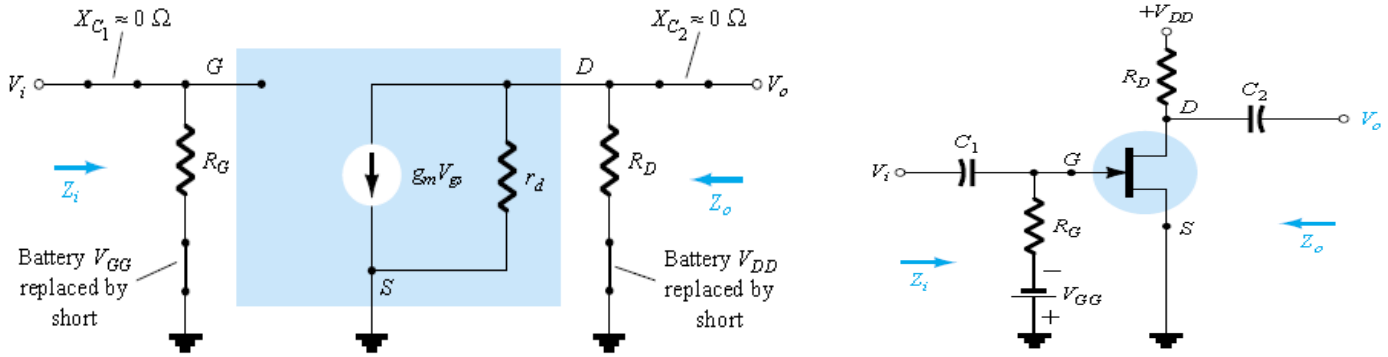


Figure 16

$$Z_i = R_G$$

$$Z_o = R_D \| r_d$$

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation is:

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

***Av*:** Solving for V_o, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $V_{gs} = V_i$

and $V_o = -g_m V_i(r_d \| R_D)$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

If $r_d \geq 10R_D$:

$$A_v = \frac{V_o}{V_i} = -g_m R_D \qquad r_d \geq 10R_D$$

The negative sign in the resulting equation for Av clearly reveals a phase shift of 180° between input and output voltages.

Example:

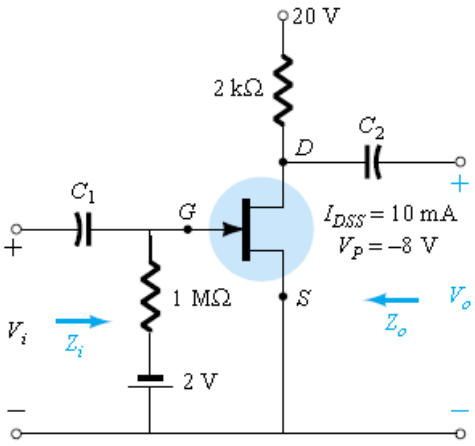
The fixed-bias configuration of Fig. bellow had an operating point defined by V_{GSQ} =-2 V and I_{DQ} = 5.625 mA, with I_{DSS} =10 mA,

V_P = -8 V, and y_{OS} = 40μS.

(a) Determine g_m. (b) Find r_d. (c) Determine Z_i.

(d) Calculate Z_o. (e) Determine the voltage gain *Av*.

(f) Determine *Av* ignoring the effects of r_d.



Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

(e) $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$

$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D resulted in a difference of 8% in solution.

- **JFET SELF-BIAS CONFIGURATION Bypassed *RS:***

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig.17 requires only one dc supply to establish the desired operating point.

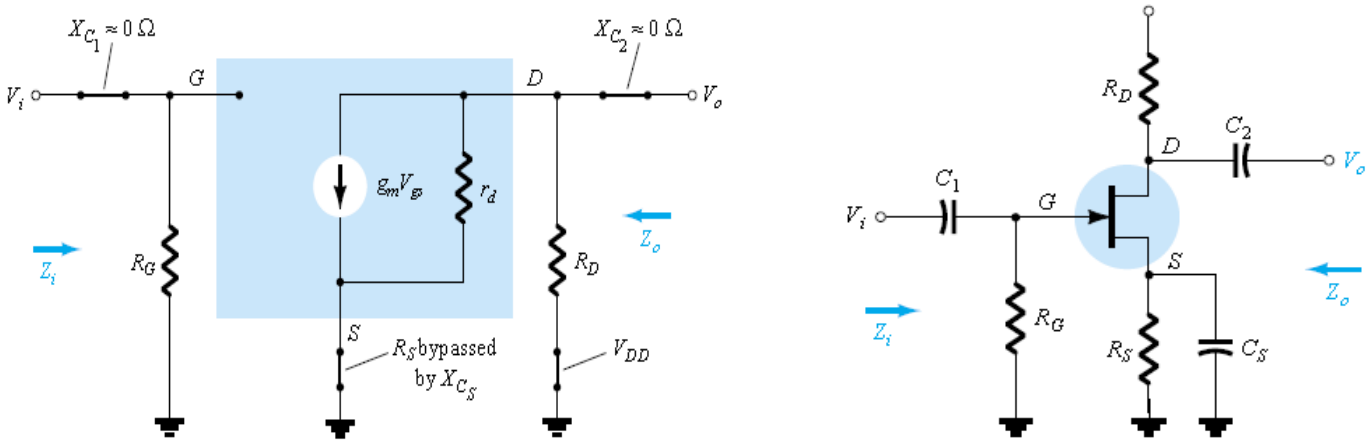


Figure 17

Since the resulting configuration of Fig.17 is the same as appearing in Fig. 16, the resulting equations *Zi*, *Zo*, and *Av* will be the same.

- **Unbypassed *RS***

If C_S is removed from Fig 17, the resistor R_S will be part of the ac equivalent circuit as shown in Fig.18. In this case, there is no obvious way to reduce the network to lower its level of complexity.

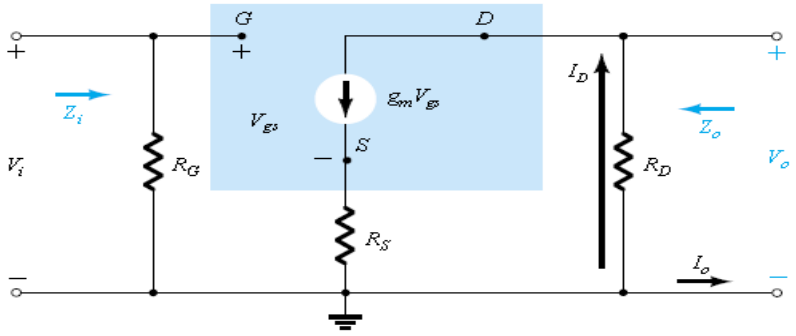


Figure 18

$$Z_i = R_G$$

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \qquad r_d \geq 10(R_D + R_S)$$

- **JFET VOLTAGE-DIVIDER CONFIGURATION:**

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 12. Substituting the ac equivalent model for the JFET will result in the configuration of Fig. 19.

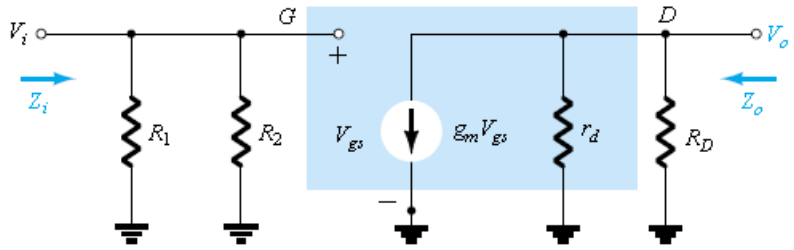


Figure 19

$$Z_i = R_1 \| R_2$$

Z_o: Setting $V_i = 0$ V will set V_{gs} and $g_m V_{gs}$ to zero and

$$Z_o = r_d \| R_D$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad r_d \geq 10R_D$$

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad r_d \geq 10R_D$$

Note that the equations for *Zo* and *Av* are the same as obtained for the fixed-bias and self bias (with bypassed R_S) configurations. The only difference is the equation for *Zi*, which is now sensitive to the parallel combination of R_1 and R_2.

Operational Amplifiers

- **Introduction:**

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain. As shown in Fig. 1 each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (-) input.

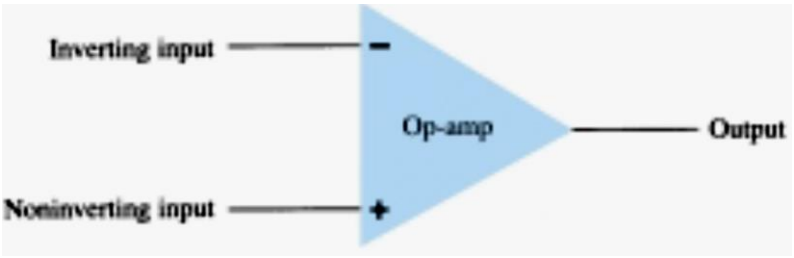


Figure 1

The ac equivalent circuit of the op-amp is shown in Fig.2

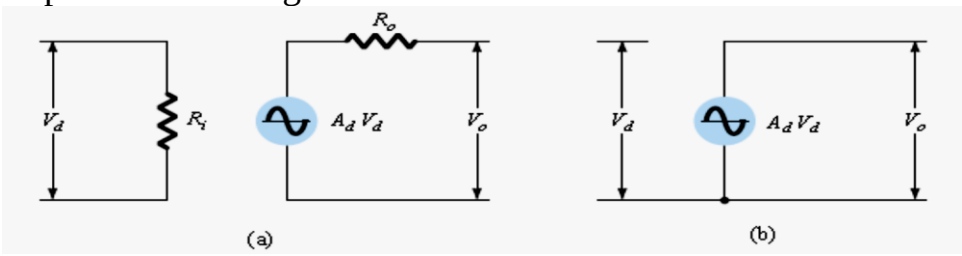


Figure2: Ac equivalent of op-amp circuit: (a) practical; (b) ideal.

- **Basic Op-Amp**
- **Inverting Amplifire:**

The basic circuit connection using an op-amp is shown in Fig. 3. The circuit shown provides operation as a constant-gain multiplier. An input signal, V_1, is applied through resistor R_1 to the minus input. The output is then connected back to the same minus input through resistor R_f. The plus input is connected to ground.

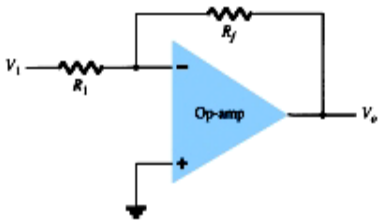


Figure 3

Fig. 4: shows the op-amp replaced by its ac equivalent circuit.

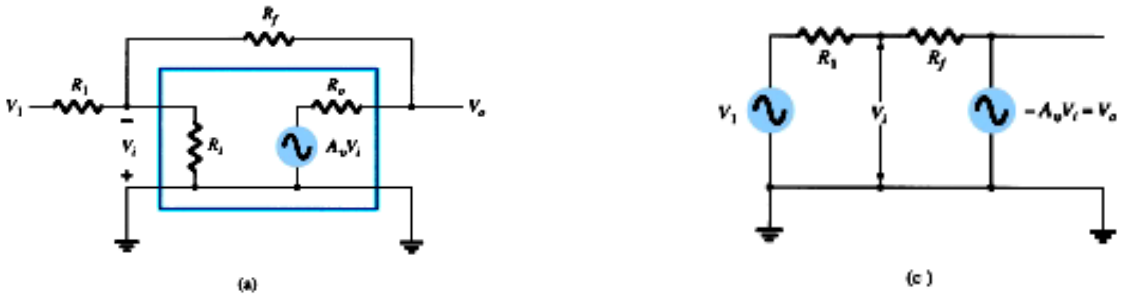


Figure 4: Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit.

Using superposition, and solve for V_1:
For source V_1 only ($-A_v V_i$ set to zero):

$$V_{i_1} = \frac{R_f}{R_1 + R_f} V_1$$

For source $-A_v V_i$ only (V_1 set to zero):

$$V_{i_2} = \frac{R_1}{R_1 + R_f} (-Av\, Vi)$$

The total voltage V_i is then:

$$V_i = V_{i_1} + V_{i_2} = \frac{R_f}{R_1 + R_f} V_1 + \frac{R_1}{R_1 + R_f} (-Av\, Vi)$$

Which can be solved for V_i as

$$V_i = \frac{R_f}{R_f + (1 + Av)R_1} V_1$$

If $Av \gg 1$ and $AvR_1 \gg R_f$, as is usually true, then:

$$V_i = \frac{R_f}{AvR_1} V_1$$

Solving for V_o/V_i, we get:

$$\frac{V_o}{V_i} = \frac{-Av\, Vi}{V_i} = \frac{-AvR_f\, V_1}{V_i AvR_1} = \frac{-R_f\, V_1}{V_i R_1}$$

So that:

$$\frac{V_o}{V_i} = \frac{-R_f}{R_1}$$

The result, in that last equation, shows that the ratio of overall output to input voltage is dependent only on the values of resistors R_1 and R_f —provided that A_v is very large.

- **Noninverting Amplifier:**

The connection of Fig. 5 shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability.

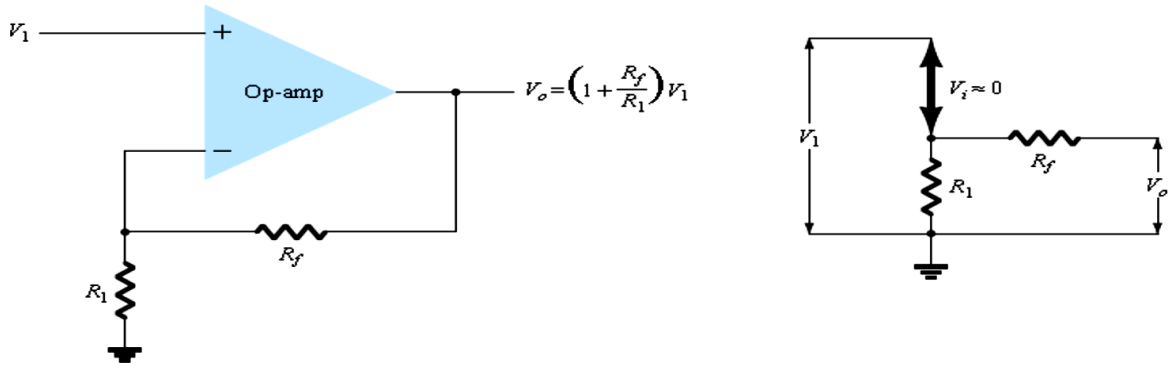


Figure 5

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

which results in

$$\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

The unity-follower circuit, and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.

- **Summing Amplifier:**

Probably the most used of the op-amp circuits is the summing amplifier circuit shown in Fig. 6. The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain factor.

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

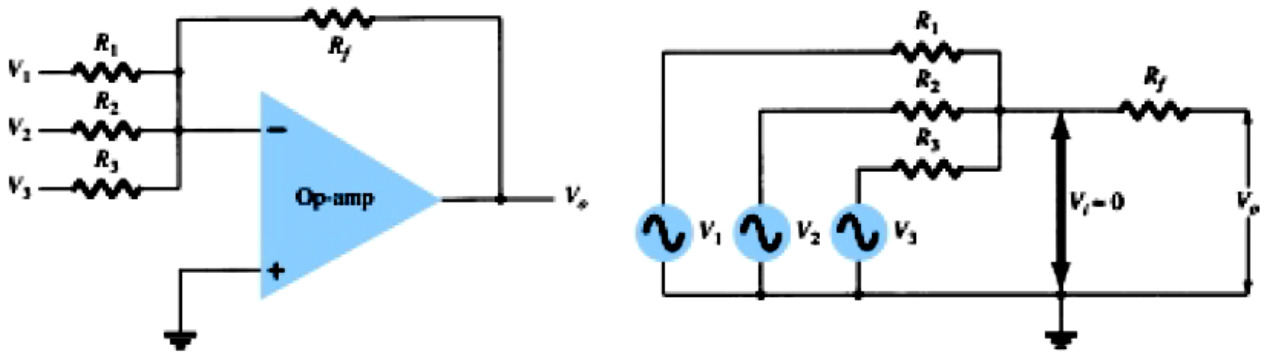


Figure 6

Example:

Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use $R_f = 1\ \text{M}\Omega$ in all cases.

(a) $V_1 = +1\ \text{V}$, $V_2 = +2\ \text{V}$, $V_3 = +3\ \text{V}$, $R_1 = 500\ \text{k}\Omega$, $R_2 = 1\ \text{M}\Omega$, $R_3 = 1\ \text{M}\Omega$.
(b) $V_1 = -2\ \text{V}$, $V_2 = +3\ \text{V}$, $V_3 = +1\ \text{V}$, $R_1 = 200\ \text{k}\Omega$, $R_2 = 500\ \text{k}\Omega$, $R_3 = 1\ \text{M}\Omega$.

$$\text{(a)}\ V_o = -\left[\frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+1\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+2\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+3\ \text{V})\right]$$

$$= -[2(1\ \text{V}) + 1(2\ \text{V}) + 1(3\ \text{V})] = -7\ \text{V}$$

$$\text{(b)}\ V_o = -\left[\frac{1000\ \text{k}\Omega}{200\ \text{k}\Omega}(-2\ \text{V}) + \frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+3\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+1\ \text{V})\right]$$

$$= -[5(-2\ \text{V}) + 2(3\ \text{V}) + 1(1\ \text{V})] = +3\ \text{V}$$

- **Integrator:**

So far, the input and feedback components have been resistors. If the feedback component used is a capacitor, as shown in Fig. 7a, the resulting connection is called an *integrator*. The virtual-ground equivalent circuit (Fig. 7b) shows that an expression for the voltage between input and output can be derived in terms of the current *I*, from input to output. Recall that virtual ground means that we can consider the voltage at the junction of *R* and *XC* to be ground (since $Vi \approx 0$ V) but that no current goes into ground at that point.

$$v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt$$

The above equation shows that the output is the integral of the input, with an inversion and scale multiplier of 1/*RC*.

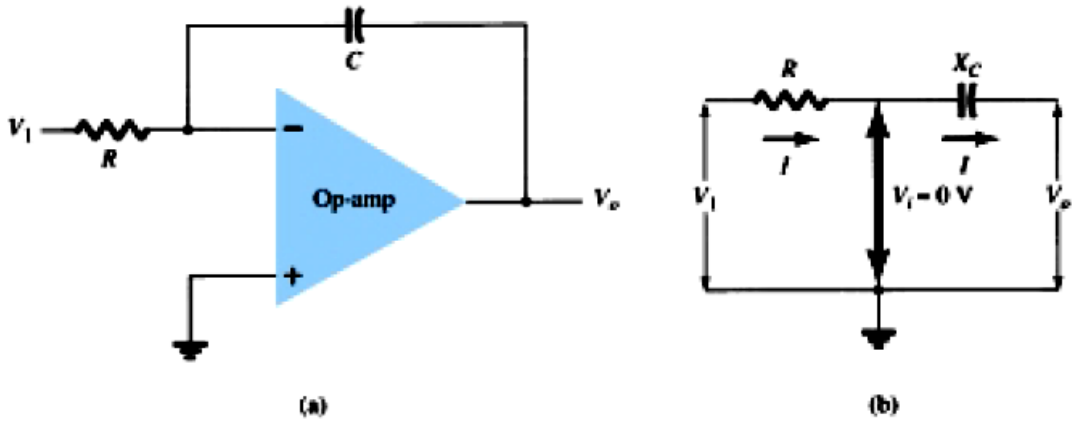


Figure 7

- **Differentiator**

A differentiator circuit is shown in Fig. 8. The resulting relation for the circuit being

$$v_o(t) = -RC\frac{dv_1(t)}{dt}$$

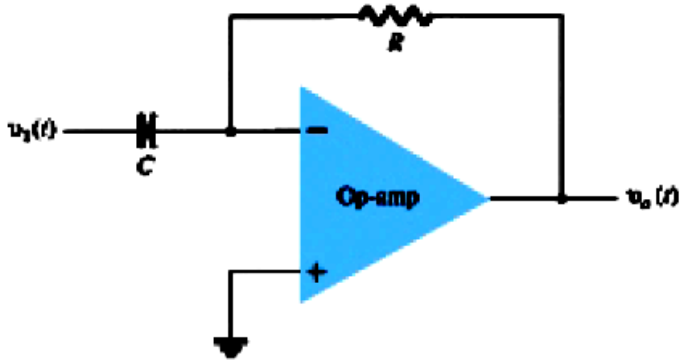


Figure 8