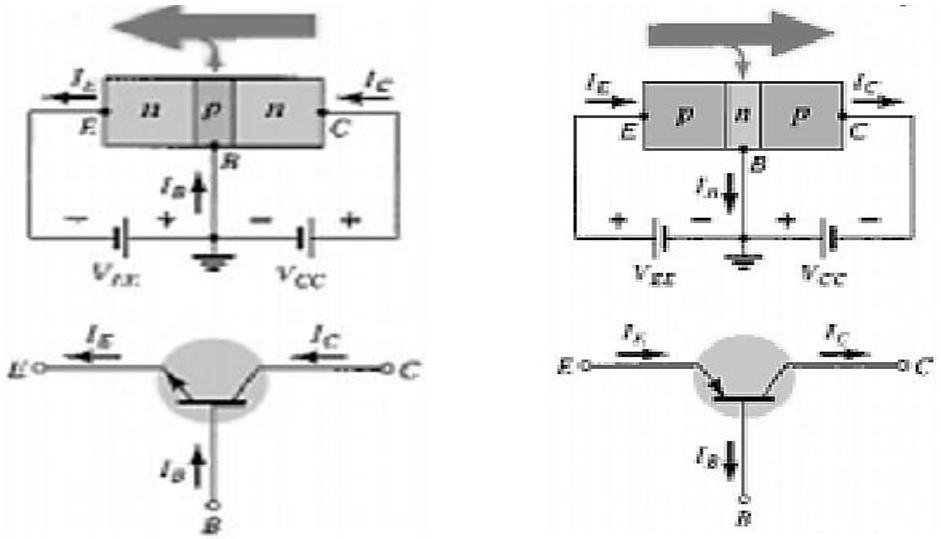
Chapter Two
Bipolar Junction Transistors (BJT)

1- Introduction:

The transistor is a three-layer semiconductor device consisting of either two n- and one p-type layers of material or two p- and one n-type layers of material. The former is called an npn transistor, while the latter is called a pnp transistor. In Fig. below both biasing potentials have been applied to a pnp transistor, with the resulting majority- and minority-carrier flow indicated.



1- Common-Base Configuration

The common-base terminology is derived from the fact that the base is common to both the input and output sides of the con-figuration. In addition, the base is usually the terminal closest to, or at, ground potential.

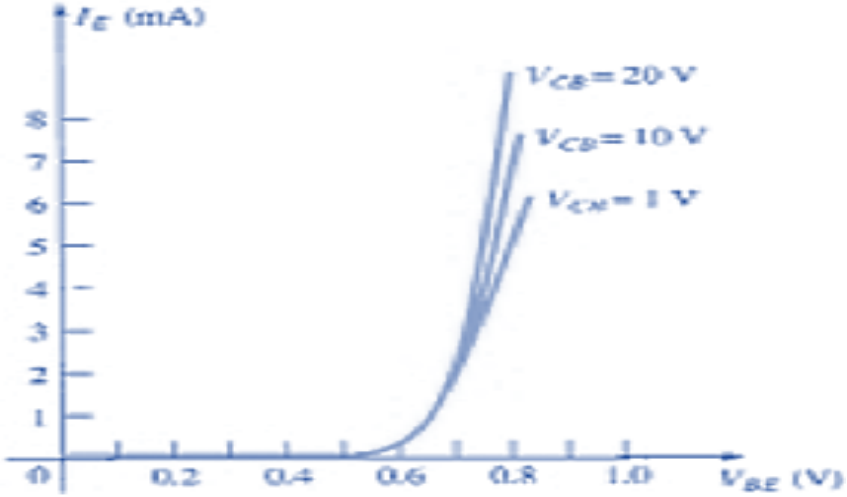
$$I_E = I_C + I_B$$

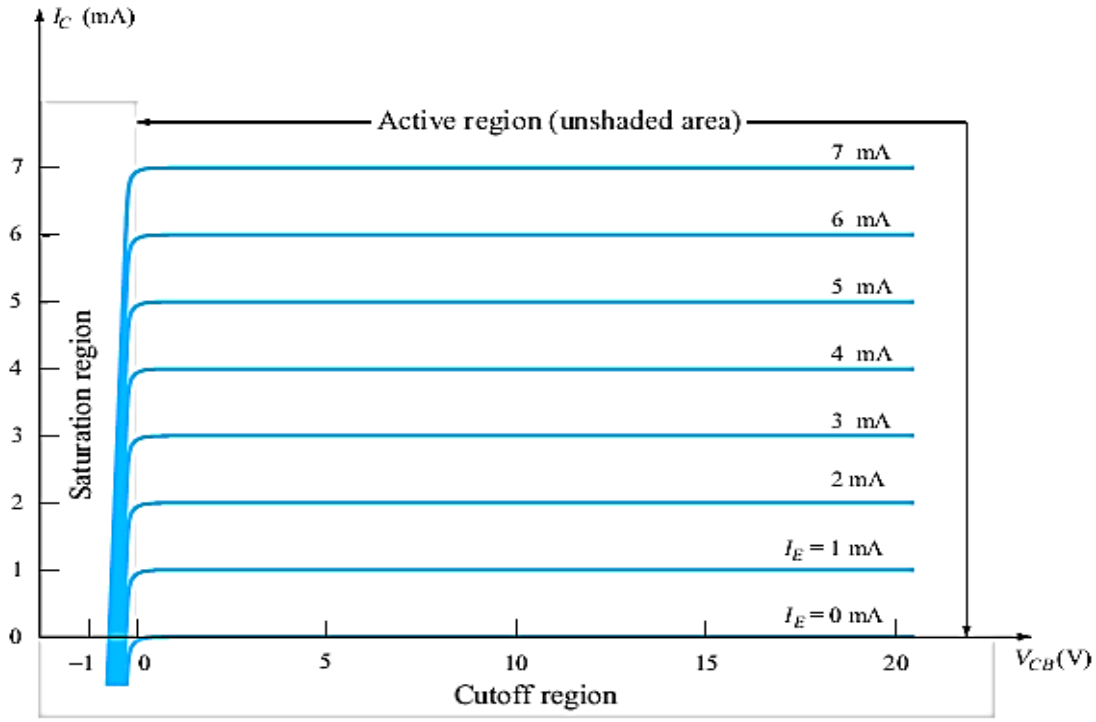
The collector current, however, is comprised of two components—the majority and mi-nority carriers. The minority-current component is called the leakage current and is given the symbol I_{CQ} (I_C current with emitter terminal Open).

To fully describe the behavior of a three-terminal device such as the common-base amplifiers requires two sets of characteristics—one for the driving pointor input parameters and the other for the outputside.

The input set for the common-base amplifier as shown below will relate an input current (I_E) to an in-put voltage (V_{BE}) for various levels of output voltage (V_{CB}).

The output set will relate an output current (I_C) to an output voltage (V_{CB}) for var-ious levels of input current (I_E) as shown.





The curves clearly indicate that a first approximation to the relationship between I_E and I_C in the active region is given by

$$I_E \cong I_C$$

A transistor is in the "on"state, the base-to-emitter voltage will be assumed to be the following:

$$V_{BE} = 0.7$$

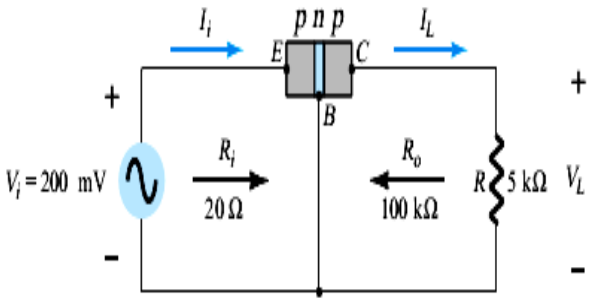
In the dc mode the levels of I_C and I_E due to the majority carriers are related by aquantity called alphaand defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E}$$

For practical devices the level of alpha typically extends from 0.90 to 0.998.

For the common-base configuration the ac input resistance is quite small and typically varies from 10 to 100Ω. The output resistance is quite high (the more horizontal the curves the higher the resistance) and typically varies from 50 k Ω to 1 M Ω (100 kΩ).

Using a common value of 20Ω for the input resistance, we find that



$$I_i = \frac{V_i}{R_i} = \frac{200\text{ mV}}{20\ \Omega} = \mathbf{10\ mA}$$

If we assume for the moment that $\alpha_{ac} = 1$ ($I_c = I_e$),

$$I_L = I_i = 10\text{ mA}$$

and

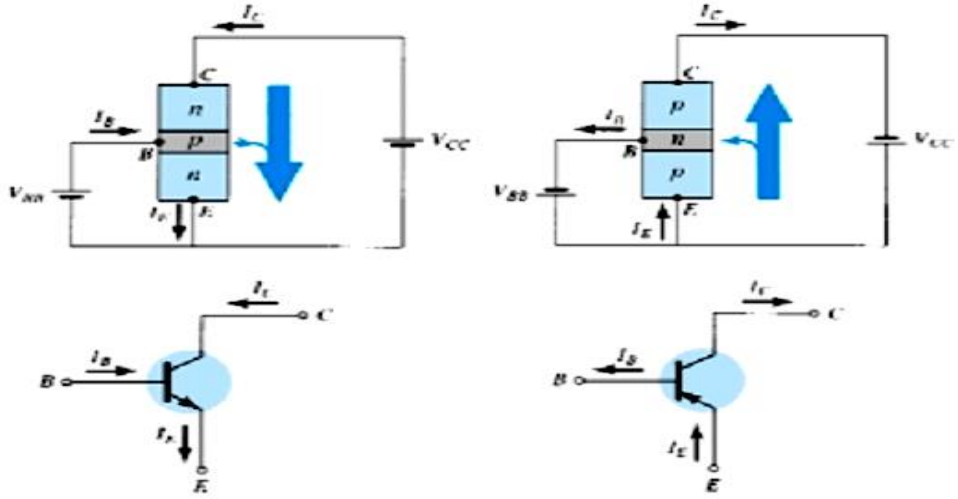
$$V_L = I_L R$$
$$= (10\text{ mA})(5\text{ k}\Omega)$$
$$= \mathbf{50\ V}$$

The voltage amplification is

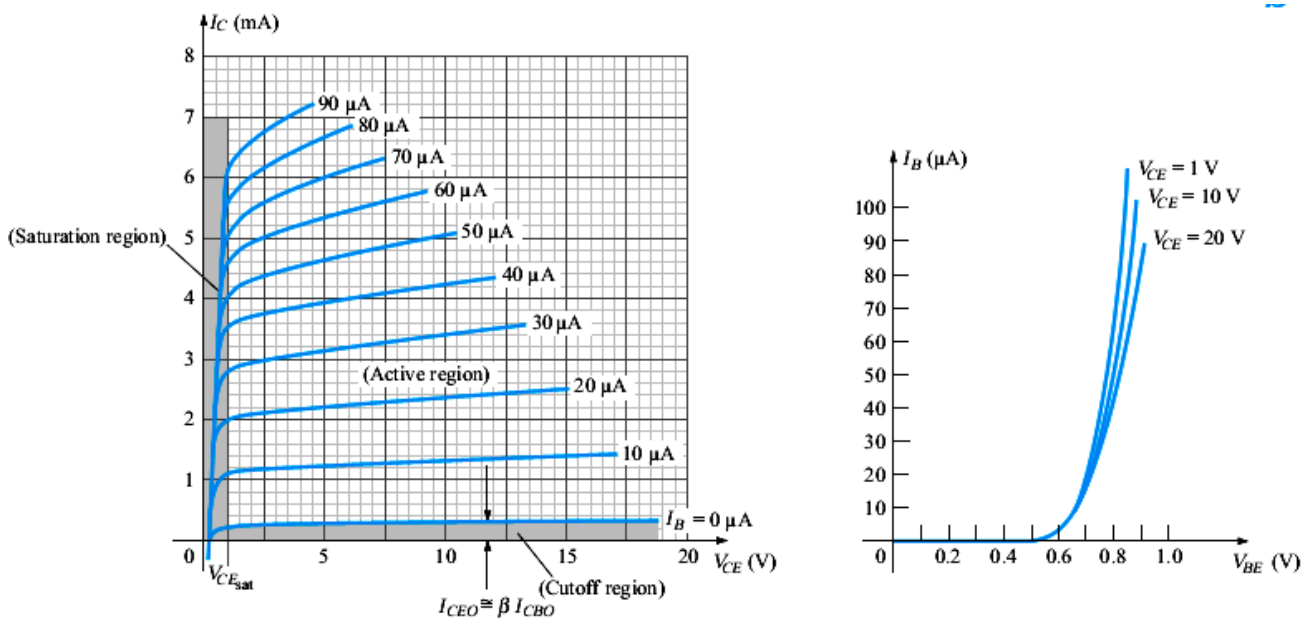
$$A_v = \frac{V_L}{V_i} = \frac{50\text{ V}}{200\text{ mV}} = \mathbf{250}$$

2- Common-Emitter Configuration

The most frequently encountered transistor configuration appears in Fig. below for the pnp and npn transistors. It is called the common-emitter configuration since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals).



For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input volt-age (V_{BE}) for a range of values of output voltage (V_{CE}).



In the dc mode the levels of I_C and I_B are related by a quantity called beta and defined by the following equation:

$$\beta_{dc} = \frac{I_C}{I_B}$$

For practical devices the level of typically ranges from about 50 to over 400, with most in the midrange.

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C/I_B$ we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$we have

$I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$

we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by I_C will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{\beta + 1}}$$

or

$$\boxed{\beta = \frac{\alpha}{1 - \alpha}}$$

$$\boxed{I_C = \beta I_B}$$

and since

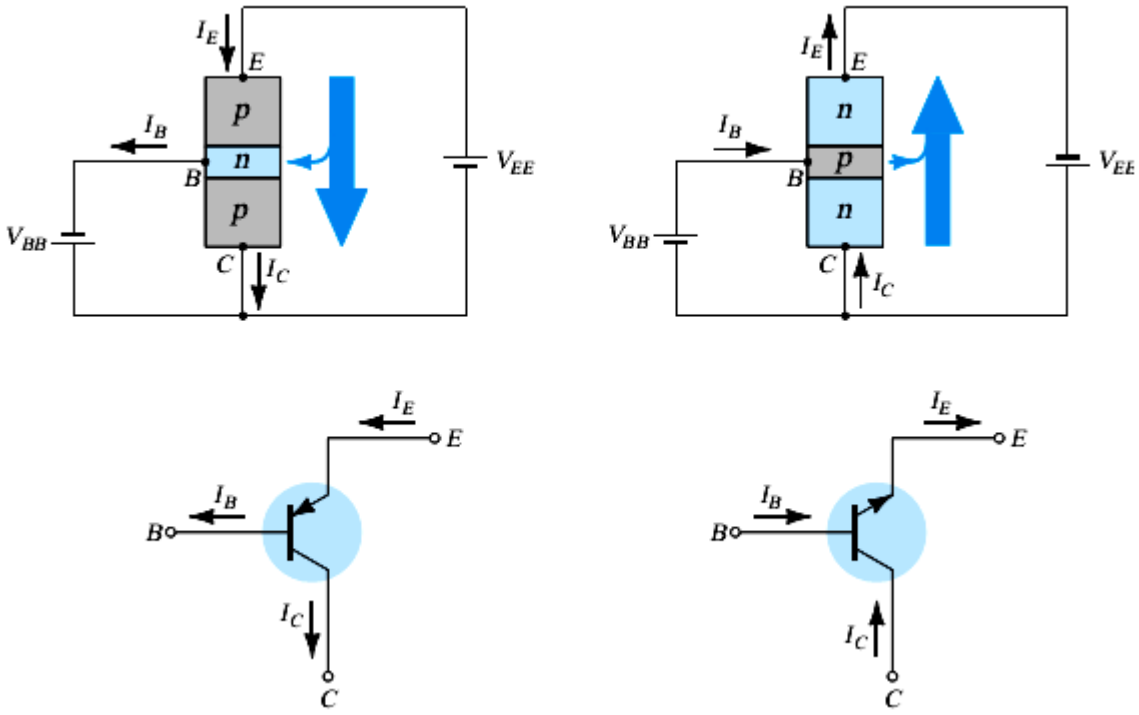
$$I_E = I_C + I_B$$
$$= \beta I_B + I_B$$

we have

$$\boxed{I_E = (\beta + 1) I_B}$$

3- Common-Collector Configuration

The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

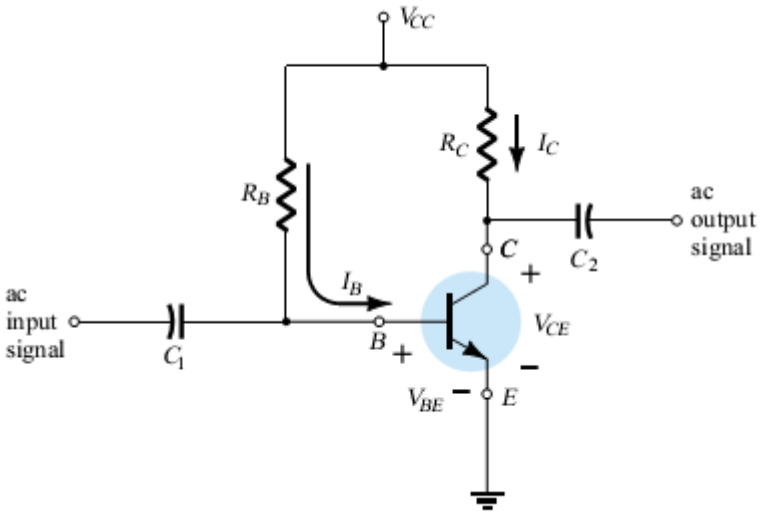


For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{CE} for a range of values of I_B. The input current, therefore, is the same for both the common-emitter and common-collector characteristics.

DC Biasing—BJTs

1- Fixed-Bias Circuit

The fixed-bias circuit of Fig. below provides a relatively straightforward and simple introduction to transistor dc bias analysis. Even though the network employs an npn transistor, the equations and calculations apply equally well to a pnp transistor con-figuration merely by changing all current directions and voltage polarities.



Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Applying Kirchhoff's voltage law in the clockwise direction

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

As a brief review of single- and double-subscript notation recall that

$$V_{CE} = V_C - V_E$$

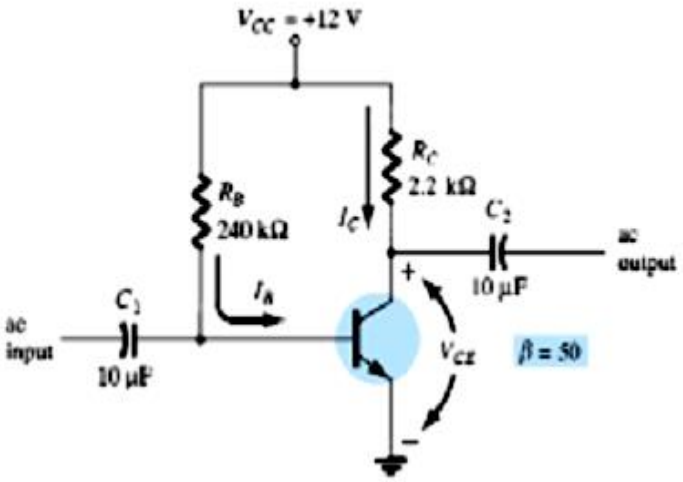
But in this case, since $V_E = 0$ V, we have

$$V_{CE} = V_C$$

In addition $V_{BE} = V_B - V_E$ then $V_{BE} = V_B$

Example: *Determine the following for the fixed-bias configuration of Fig. below.*

(a) I_{BQ} *and* I_{CQ} *(b)* V_{CEQ} *(c)* V_B *and* V_C. *(d)* V_{BC}.



(a) $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$$

$$I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$$

(b) $$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$$
$$= \mathbf{6.83\ V}$$

(c) $V_B = V_{BE} = \mathbf{0.7\ V}$

$V_C = V_{CE} = \mathbf{6.83\ V}$

(d) Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

The saturation current for the fixed-bias configuration is

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

Where $V_{CE} = 0$ for this case

Load-Line Analysis: The network of Fig. below establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C$$

If we choose I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting I_C= 0 mA, we find that

$$V_{CE} = V_{CC}|_{I_C=0\text{ mA}}$$

If we now choose V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0\text{ V}}$$

Example: *Given the load line of Fig. below and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.*

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\text{ V}$$

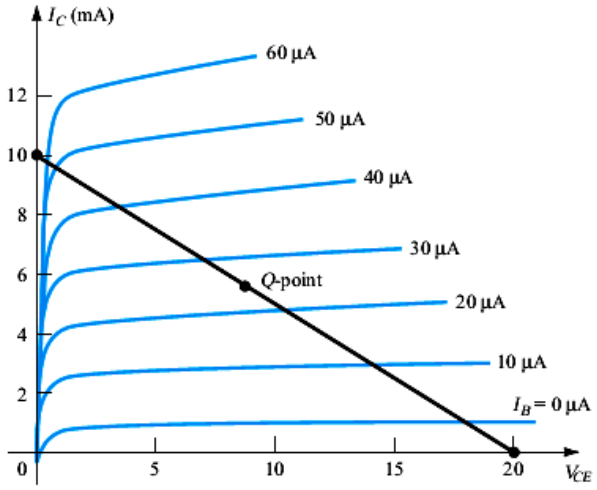
and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\text{ V}}{10\text{ mA}} = \mathbf{2\ k\Omega}$$

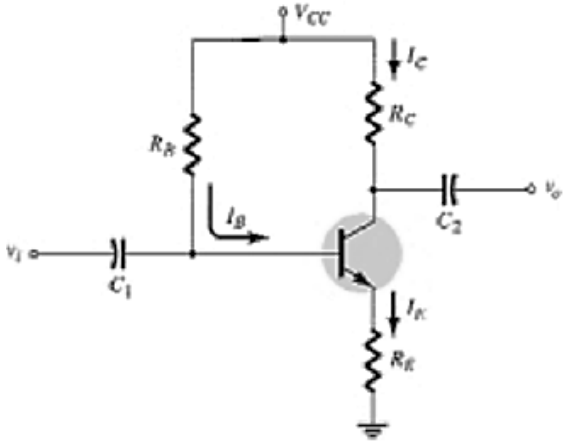
$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{ V} - 0.7\text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$



The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.



The base–emitter loop of the network is:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$we\ have\ I_E = \beta I_B + I_B = (\beta + 1) I_B$$

$$+V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$V_{CC} - V_{BE} = I_B R_B + (\beta + 1) I_B R_E$$

Then $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$

Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is reflected back to the input base circuit by a factor $(\beta + 1)$.

$$R_i = (\beta + 1) R_E$$

Writing Kirchhoff's voltage law for collector-emitter loop in the clockwise direction will result in

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

Substituting $I_C \cong I_E$

$$-V_{CC} + I_C R_C + V_{CE} + I_C R_E = 0$$

$$V_{CE} - V_{CC} + I_C (R_C + R_E) = 0$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$\boxed{V_E = I_E R_E}$$

while the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and $$\boxed{V_C = V_{CE} + V_E}$$

or $$\boxed{V_C = V_{CC} - I_C R_C}$$

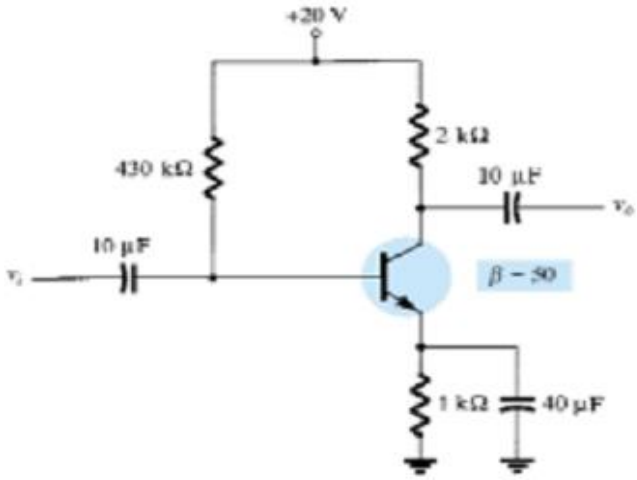
The voltage at the base with respect to ground can be determined from

$$\boxed{V_B = V_{CC} - I_B R_B}$$

or $$\boxed{V_B = V_{BE} + V_E}$$

Example:

For the emitter bias network of Fig.
(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.
(e) V_E.
(f) V_B.
(g) V_{BC}.



(a) $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

(b) $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\ mA}$

(c) $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$= \mathbf{13.97\ V}$

(d) $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\ V}$

(e) $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\ V}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.01\ V}$

(f) $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\ V}$

(g) $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\ V}$ (reverse-biased as required)

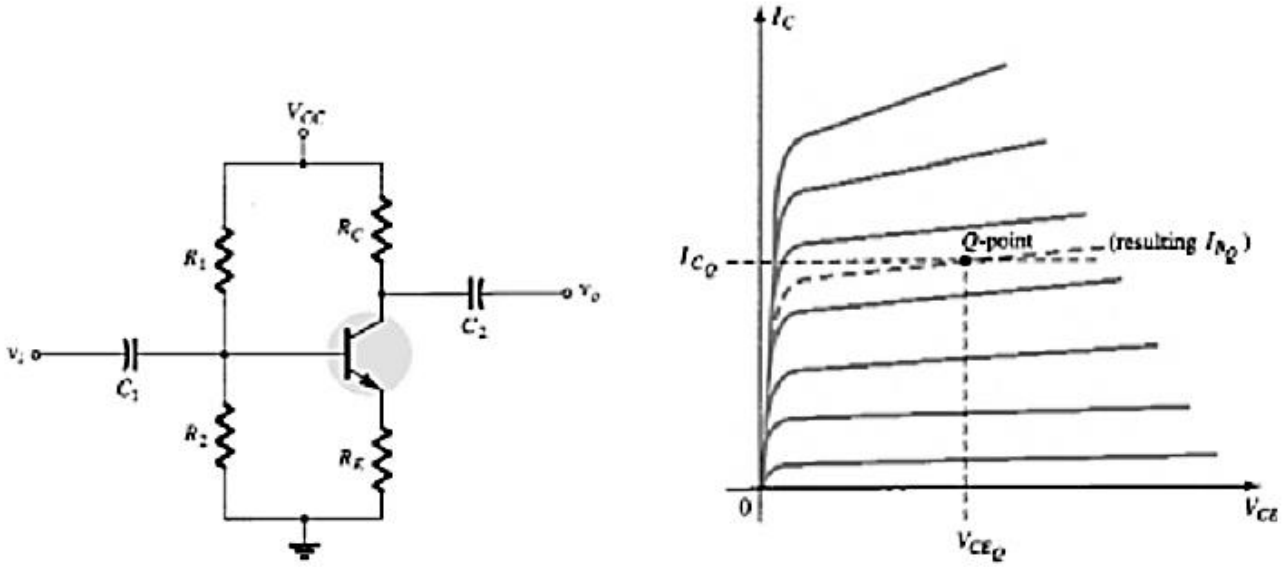
The collector saturation level or maximum collector current for an emitter-bias de-sign can be determined

$$I_{Csat} = \frac{V_{CC}}{R_C + R_E}$$

2- Voltage-Divider Bias:

The voltage-divider bias configuration of Fig. below is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{CQ} and V_{CEQ} can be almost totally independent of beta.

There are two methods that can be applied to analyze the voltage-divider configuration.



Exact Analysis:

The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

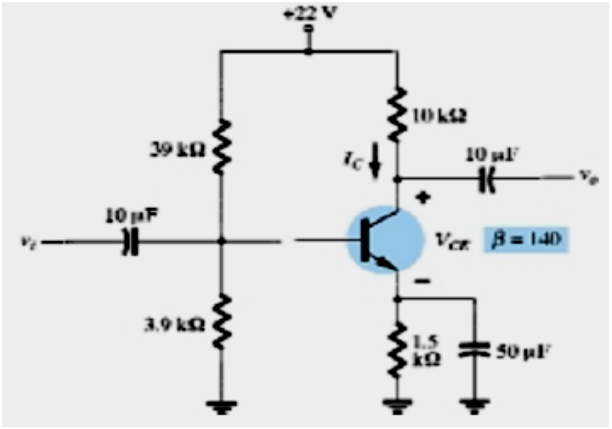
$$R_{Th} = R_1 \| R_2$$

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

Example: *Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig.*



$$R_{Th} = R_1 \| R_2$$

$$= \frac{(39\ \text{k}\Omega)(3.9\ \text{k}\Omega)}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 3.55\ \text{k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 2\ V$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2\ \text{V} - 0.7\ \text{V}}{3.55\ \text{k}\Omega + (141)(1.5\ \text{k}\Omega)} = \frac{1.3\ \text{V}}{3.55\ \text{k}\Omega + 211.5\ \text{k}\Omega}$$

$$= 6.05\ \mu A$$

$$I_C = \beta I_B$$

$$= (140)(6.05\ \mu\text{A})$$

$$= \mathbf{0.85\ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\ \text{V} - (0.85\ \text{mA})(10\ \text{k}\Omega + 1.5\ \text{k}\Omega)$$

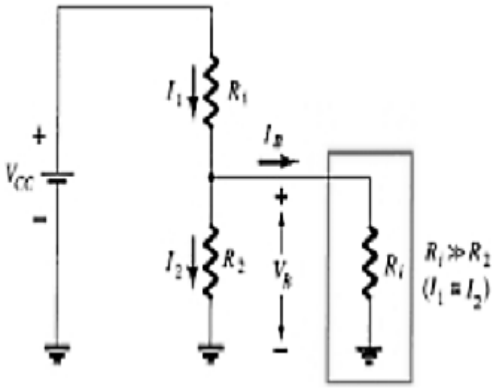
$$= 22\ \text{V} - 9.78\ \text{V}$$

$$= \mathbf{12.22\ V}$$

Approximate Analysis:

The input section of the voltage-divider configuration can be represented by the network of Fig.below. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E.

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$



The condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_E \geq 10R_2$$

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$

$$I_{C_Q} \cong I_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but since $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

H.W: *Repeat the analysis of previous example using the approximate technique, and compare solutions for* I_{CQ} *and* V_{CEQ}

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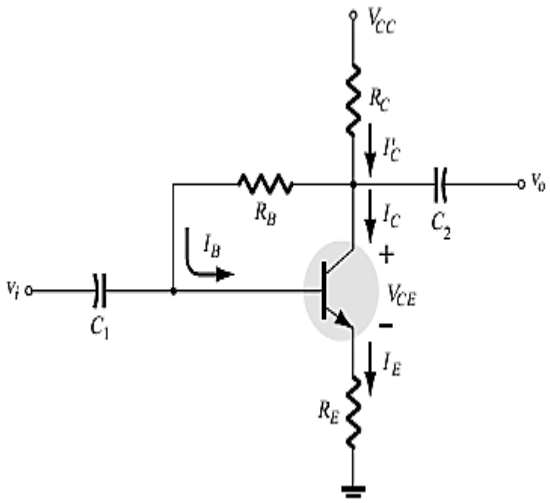
3- DC Bias with Voltage Feedback:

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig.below. Although the Q-point is not totally in-dependent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations.



Writing Kirchhoff's voltage law around the base-emitter loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Substituting $I'_C \cong I_C = \beta I_B$ *and* $I_E \cong I_C$

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

$$V_{CC} - \beta I_B(R_C + R_E) - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{\beta(R_C + R_E) + R_B}$$

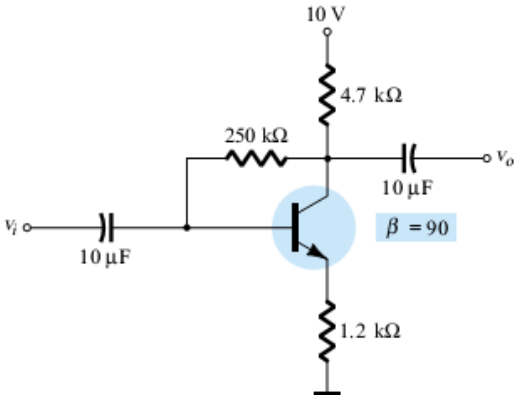
In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

Applying Kirchhoff's voltage law around the collector–emitter loop in the clockwise direction will result in

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Example: *Determine the quiescent levels of I_{CQ} and V_{CEQ} for the network of Fig. shown.*



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 6.31\text{ V}$$

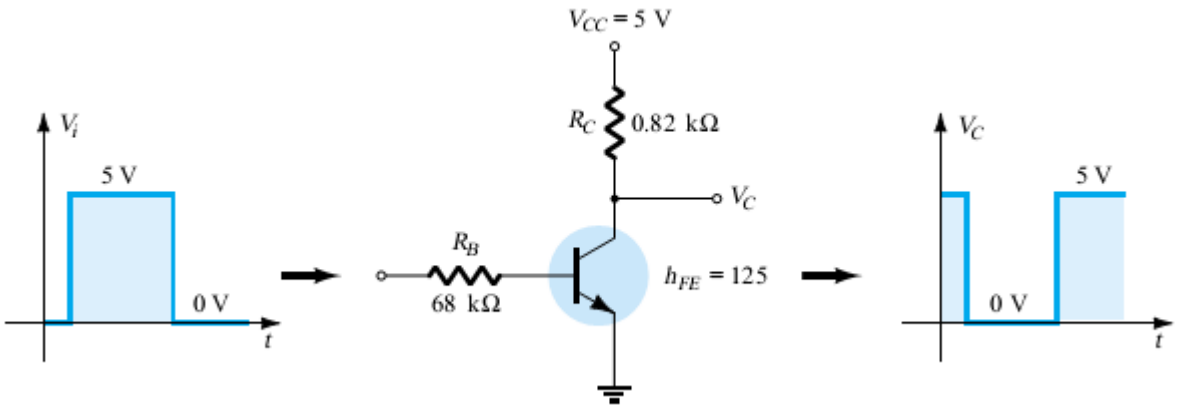
$$= \mathbf{3.69\text{ V}}$$

H.W: *Repeat the previous Example using a beta of 135.*

It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

4-Transistor Switching Networks:

The application of transistors is not limited solely to the amplification of signals. Through proper design it can be used as a switch for computer and control applications.



Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line.

The saturation level for the collector current is defined by

$$I_{Csat} = \frac{V_{CC}}{R_C}$$